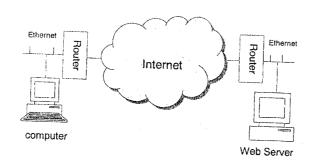
國立中央大學九十三學年度碩士班研究生入學試題卷 共2頁 第12頁

所別: 通訊工程學系碩士班 丙組 科目: 計算機系統

1. Explain

- (1) Why cyclic redundancy checks (CRC) can detect more errors than a simple checksum? (6%)
- (2) The strength and weakness of CSMA/CD and token ring protocols, and why they are inappropriate for use in the wide area networks (WAN)? (7%)
- (3) TCP v.s. UDP. (5%)
- (4) Time Division Multiplexing. (5%)
- 2. Assume that a computer is browsing a Web server as shown in the following figure, draw the protocol stack used on the routers, computer, and the Web server. And describe which places may cause congestion. (15%)



- 3. What is the difference between IPv6 and the current IPv4? And why does IPv6 use separate extension header? (12%)
- 4. Does a computer with higher MIPS (millions of instructions per second) always have a faster response time than a computer with lower MIPS when executing the same program? Why? (8%)
- 5. Consider a computer equipped with 2M Bytes main memory and 128K Bytes cache, and the size of each block is assigned as 64 Bytes. Please depict the arrangement of address bits (thus, Tag bits, block/set bits, displacement/offset bits) for the following conditions.
 - (1) Direct-mapped cache (6%)
 - (2) Fully associative-mapped cache (6%)
 - (3) 4-way set associative-mapped cache (thus, each set has 4 blocks) (8%)



國立中央大學九十三學年度碩士班研究生入學試題卷 共 2 頁 第 2 頁

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- 6. Consider a non-pipelined machine with 5 execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, and 50 ns.
 - (1) What is the instruction latency of this machine. (3%)
 - (2) How much time does it take to execute 100 instructions? (3%)
 - (3) Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 5ns of overhead to each execution stage. Then, how much time does it take to execute 100 instructions (ignoring any hazard)? (8%)
- 7. Explain
 - (1) CPI (4%)
 - (2) RISC (4%)

