1. (20%)

For the high-frequency equivalent circuit model of the n-channel MOSFET as shown in Fig 1, (1) derive a formula for the MOSFET f_T, assuming Cgd is small, (7%) (2) if the overlap component of Cgs is negligibly small and $C_{gs} \gg C_{gd}$, show that $f_T \approx \frac{3}{2\pi L}\sqrt{\frac{\mu_n I_D}{2C_{ox}WL}}$ (7%) (3) evaluate f_T for MOSFET with L=2 μ m operated at $(V_{gs} - V_t)$=0.5 V, if $\mu_n = 400\ cm^2/V \cdot s$ (6%)

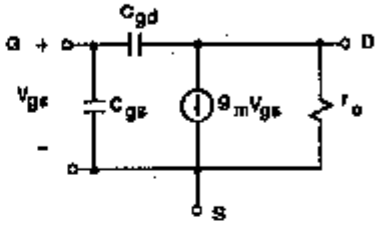


Fig 1

2. (20%)

(1) Find the equivalent hybrid-π model of the Darlington circuit as shown in Fig 2, assuming Q1 and Q2 have the same β, expressing the overall r'_π and g'_m values in terms of $r_{\pi 1}$, $r_{\pi 2}$, g_{m1} and g_{m2} (10%) (2) Understanding that the $r_{\pi 2}$ and g_{m2} of Q2 differ from $r_{\pi 1}$ and g_{m1} of Q1 in magnitudes, if $\beta \gg 1$, find a corresponding approximate hybrid-π model. (10%)

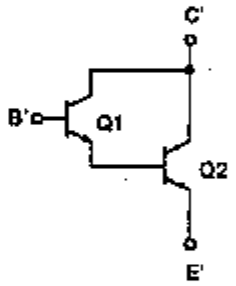


Fig 2

3. (28%)

For the OP-amplifier as shown in Fig 3 (a), if the voltage gain of the OP is modeled as

$$A_v(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{100}{(1+\frac{s}{10})(1+\frac{s}{10^3})}(V/V)$$

, the input impedance of the OP $\rightarrow \infty$, and the output impedance of the OP $\rightarrow 0$. (1) If this OP is employed in a feedback amplifier as shown in Fig 3 (b), what kind of feedback topologies (series-shunt, shunt-shunt, shunt-series, series-series) is utilized? (4%) If this OP is employed in a feedback amplifier as shown in Fig 3 (c), what kind of feedback topologies (series-shunt, shunt-shunt, shunt-series, series-series) is utilized (4%)?

For the following questions, consider the feedback amplifier shown in Fig 3(c) ONLY, and $R_1 = 1\ k\ \Omega$, $R_2 = 4\ k\ \Omega$. (2) Derive the DC voltage gain of the feedback amplifier shown in Fig 3(c) (7%). (3) What is the 3-dB bandwidth of the feedback amplifier shown in Fig 3(c) (5%)? (4) If $R_1 = 1\ k\ \Omega$, what should be R_2 if the designed feedback amplifier [as shown in Fig 3(c)] has a 90° phase margin? (8%)

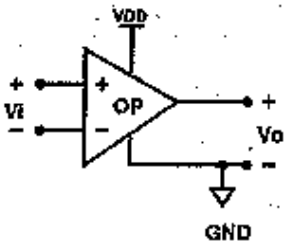


Fig 3 (a)

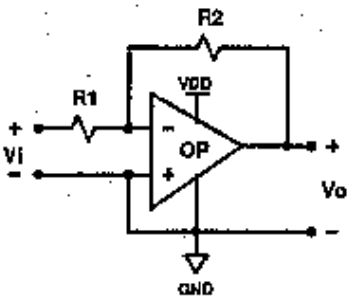


Fig 3 (b)

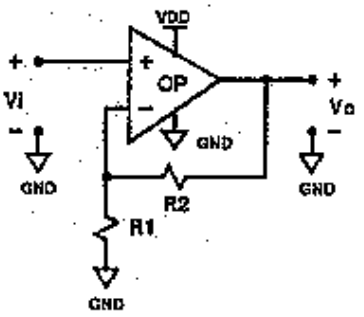


Fig 3 (c)

4. (20%)

Consider the fully differential amplifier as shown in Fig 4. Assume the current source $I_{bias} = 1mA$, thermal voltage $V_T = 25mV$, the current source has a output impedance R_S of 50 k Ω, Q_1 and Q_2 are identical, $\beta_1 = \beta_2 = 100$, $r_{o1} = r_{o2} = r_{\mu 1} = r_{\mu 2} = \infty$, $R_{C1} = R_{C2} = 10k\ \Omega$, $R_{L1} = 20\ k\Omega$, $R_{L2} = 5\ k\Omega$. $R_{E1} = R_{E2} = 50\ \Omega$. (1) Derive the differential mode voltage gain $\frac{V_o}{V_i}$. (6%) (2) Sketch the common mode half circuit. (6%) (3) If $R_{C1} = 10.1\ k\ \Omega$ and $R_{C2} = 9.9\ k\ \Omega$, what is the input offset voltage ? (8%)

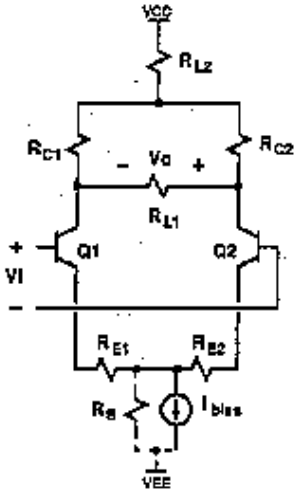


Fig 4

5. (12%)

Consider the domino logic circuit as shown in Fig 5(a), describe the boolean function O = f(A, B, C, D) (3%) and Y = f(A, B, C, D, E) (4%) when clock ϕ is high . Fig 5 (b) shows a typical static CMOS NAND gate, sketch a static CMOS logic circuit that realize the boolean function of Y = (AB+CD)E + FG (5%).

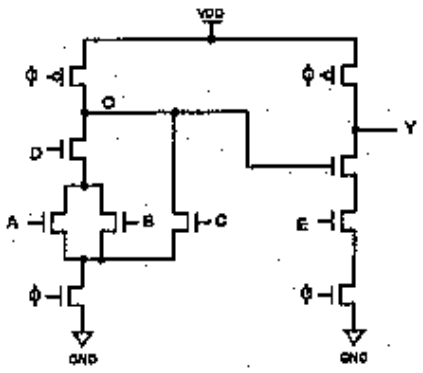
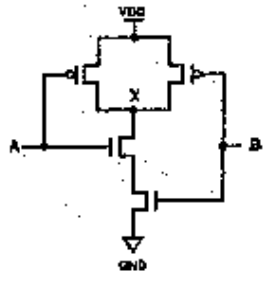


Fig 5 (a)



Typical static CMOS NAND gate
Fig 5 (b)

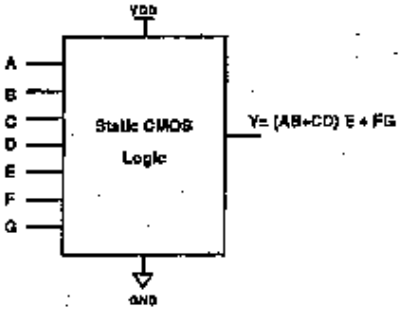


Fig 5 (c)