# 國立中央大學98學年度碩士班考試入學試題卷

所別：資訊工程學系碩士班　科目：作業系統與計算機組織　共 4 頁 第 1 頁

所別：軟體工程研究所碩士班　＊請在試卷答案卷（卡）內作答



1. (Multiple choices question) (8 points)
   A storage cell in a DRAM:
   (a) is volatile. (b) is a capacitor. (c) is cheaper than cells in a SRAM. (d) is a latch. (e) must be refreshed regularly. (f) is smaller than cells in a SRAM. (g) is typically used for cache RAM. (h) is faster than an SRAM.

2. (Multiple choices question) (4 points)
   Choose the correct description for a RISC processor:
   (a) RISC processors have more specialized registers rather than general purpose.
   (b) RISC processors have a very limited number of addressing modes.
   (c) RISC processors using 2-way pipelined timing (only two instructions can be in the pipe at any on time) do so in order to avoid two simultaneous memory accesses.
   (d) RISC processors use a fixed instruction length.

3. (7 points) The chip select definition shown as Fig.1, (a) what are the high and low addresses (in hexadecimal) of the memory range defined with this chip select? (3 points) (b)how big is the memory chip that uses this chip select? (2 points)(c) how big is the memory space of the processor whose address lines are used for the chip select? (2 points)

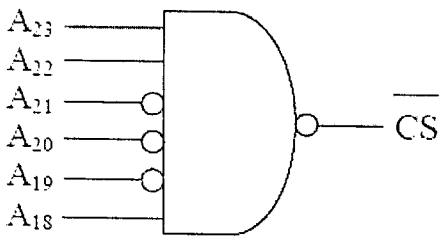



Fig.1 Chip select

4. (6 points) The code below uses a three-operand instruction:
   ```
   ADD C,A,B ; C = A + B
   ```
   In the space below, write three short programs that do exactly the same thing, one with two-operand instructions, one with one-operand instructions, and one with zero-operand instructions. For fitting the need of the instruction, please use register names R1, R2, etc.

參考用

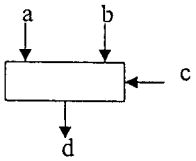
注意：背面有試題

| *Two operand instructions* | *One operand instructions* | *Zero operand instructions* |
|---|---|---|
| | | |

5. (4 points.) IEEE754
   Please show the IEEE754 single precision floating-point representation of "785.3125".

6. (4 points.) Memory hierarchy
   For a 32-bit address, determine the total number of bits (including the tag bits, data, dirty bits) to implement a 2-way set-associative cache with 128KB of data and two-word (64 bits) blocks. (4 pts.)

7. (10 points.) ALU
   a. Design a one-bit ALU that can support AND/NAND, OR/NOR, ADD and 2's complement subtraction. Describe what should be added to make it work as the MSB and LSB, if we need to construct a multi-bit ALU. (5 pts.)
   b. Try to use the following multiplexers (i.e., c=0, d=a, and c=1 d=b) to design a combinational shifter that can shift 0~3 bits. Assume that both the input data and output data of your shifter have 4 bits. 2 control bits are used to determine the shift amount. (5 pts.)




8. (7 points.) Carry Look-ahead Adder (CLA)
   Please use 4-bit CLA's to design an efficient 12-bit CLA. Please draw the block diagram first and then describe how signals are generated/ processed step by step to determine the last Carryout (CarryOut11) in the following example:
   x:0001 1010 0011
   y:1110 0101 1110

參考用

9. (10 points)
   (a.) What are the various components of interrupt and dispatch latency?
   (b.) What are the various kinds of performance overheads associated with servicing an interrupt?

10. (5 points) Using the program shown in the following list, explain what will be output at Line A?

Please give your reason .

```
#include <sys/types.h>
#include <stdio.h>
#include <unistd.h>
int value   = 10;

int main( )
{
pid_t     pid;
   pid = fork ( );
   if (pid == 0 ) {
      value +=15;
   }
else if (pid > 0) {
      wait (NULL);
      printf("PARENT: value = %d", value); /* LINE A */
      exit(0);
      }
}
```

11. (10 points) How many page faults occur for these page-replacement algorithm, (1) FIFO, (2) Optimum, (3) LRU for the following reference string, with 4 page frames?

1,2,3,4,5,3,4,1,2,6,7,8,7,8,9,6,7,9,4,5,4,5,2

12. (Multiple choices question) (10 points)
Assume there is a uni-processor system with 2 GB memory and a 500 GB disk. The OS on the machine has a demand paged virtual memory system with a replacement policy and a multi-level feedback queue (MLFQ) CPU scheduler, where the aging is implemented in the MLFQ scheduler. On the system there are two compute-intensive jobs running: Process A and Process B. Process A has working set of 79 GB while Process B has a working set of 97 MB. Assume you left the system to run for a while until it reached a steady state with both jobs running. Which statements in the following are correct?

(a) If a local replacement policy is adopted, Process B will have a higher CPU scheduling priority from the MLFQ scheduler.
(b) If a global replacement policy is adopted, page faults of Process A will increase.
(c) If a global replacement policy is adopted, priority of Process B will be lowered.
(d) If additional processors are equipped with the machine and a local replacement policy is adopted, priority relationship between the two processes will be changed.
(e) None of the above.

13. (Multiple choices question) (8 points)
Which of the following conditions would necessarily present a system that is thrashing?
(a) Paging disk is nearly 100% active
(b) CPU is 100% busy
(c) CPU is 100% idle
(d) Some processes are blocked much of the time
(e) None of the above

14. (7 points) Consider a paging system with the page table stored in memory, where a memory reference takes 100 ns. Now we add associative registers, and the time to access the associative registers is actually 2 ns. If 60 percent of all page-table references are found in the associative registers, what is the effective memory reference time?

參考用