一．Explain the following terms: (20%)

(a) Delayed load (b) Control hazard (c) Array processor (d) Associative memory (e) Cache coherence

二．(a) MIPS is used to measure the speed of a CPU. For a given program, suppose we know the Instruction Count(IC), Clock cycle time, and CPU clocks. Please define MIPS using these terms. What is the relationship between MIPS and Clock Rate which is used by a processor. (6%)

(b) A compiler designer is trying to decide between two code sequences for a particular machine. The hardware designers have supplied the following facts:

Instruction class	CPI for this instruction class
A	1
B	2
C	3

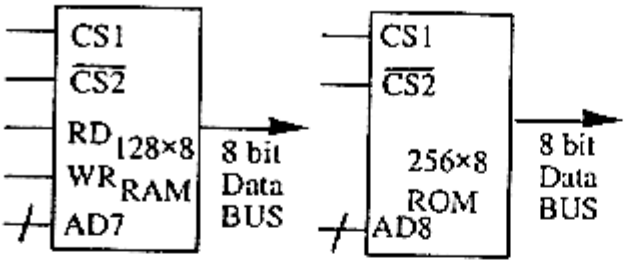
For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

	Instruction counts (inmillions) for instruction class		
Code sequence	A	B	C
1	5	1	1
2	10	1	1

Assume that the machine's clock rate is 100MHz. What is the MIPS for each sequence? Which code sequence will execute faster ? (7%)

(c) Assume an instruction cache miss rate for a MIPS program of 5% and a data cache miss rate of 10%. (Suppose the frequency of loads and stores of the program is 33%, and the frequency of other instructions is 67%.) If a machine has a CPI(clock cycles per instruction) of 4 without any memory stalls and the miss penalty is 12 cycles for all misses, determine how much faster a machine would run with a perfect cache that never missed. (7%)

三．There are two kinds of memory chip: RAM and ROM. Their block diagrams and truth table are shown in Figure 1. A microprocessor system needs 256 bytes RAM and 256 bytes ROM. It consists of RAM and ROM in Figure 1, and its Memory Address Map is shown in Figure 2. Please draw the connection among microprocessor, RAM and ROM. (20%)



Function Table:

CS1	$\overline{CS2}$	RD	WR	Function
0	0	×	×	Inhibit
0	1	×	×	Inhibit
1	0	0	0	Inhibit
1	0	0	1	Write
1	0	1	×	Read
1	1	×	×	Inhibit

CS1: chip select 1
CS2: chip select 2
Rd: read
WR: Write

Figure 1

component	Hexadecimal address	Address bus 9 8765 4321
RAM1	0000-007F	0 0xxx xxxx
RAM2	0080-00FF	0 1xxx xxxx
ROM	0100-01FF	1 xxxx xxxx

Figure 2

四. (a) For vectored interrupts, does the I/O module place the vector on the data lines or address lines ? Why ? (10%)

(b)We know there is a speed gap between CPU and main memory. Please propose three approaches to improving the gap and describe them briefly. (10%)

五. (a) Suppose two's complement is used in a number system. Please design a hardware to detect the overflow of the addition of two 8-bit. (10%)

(b) A basic microprogramming control unit is composed of the following units. Please draw the basic architecture of microprogramming control unit using block diagrams. (10%)

CM: Control Memory

UMR: Microinstruction Register

UPC: Microprogram Counter

MUX: Multiplexer

DEC: Decoder