系所別：電機工程學系　甲組　科目：電子學

乙、丙組

通訊工程學系　丙組

參考用

1. 選擇題(15 分，答錯每小題倒扣 2 分)

For the circuit shown in Fig. 1.1, let $R_1 + R_2 = 100$ kΩ, $R_D = 4$ kΩ, $R_S = 1$ kΩ, $\mu_n C_{ox} = 100$ μA/V², $(W/L)_n = 2.5$ μm/1 μm, $V_t = 1$ V, and $V_A = \infty$. There are five bias conditions available: (A) $R_1/R_2 = 10$, (B) $R_1/R_2 = 5$, (C) $R_1/R_2 = 2$, (D) $R_1/R_2 = 1$, and (E) $R_1/R_2 = 0.1$.

(1) Which condition could provide the maximum voltage gain v_o/v_i? (5 分)

(2) Which condition could provide the maximum output symmetrical signal swing? (5 分)

(3) Which condition could cause the minimum dc power dissipation in the MOS transistor? (5 分)

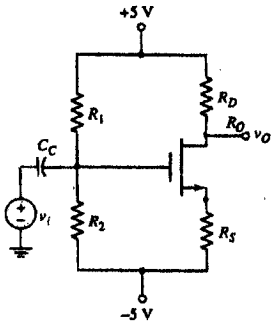

Fig. 1.1

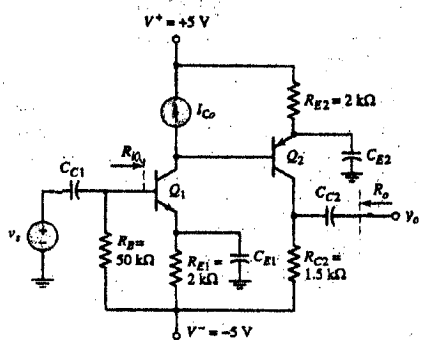

Fig. 2(a)

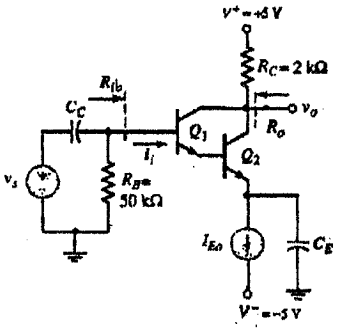

Fig. 2(b)

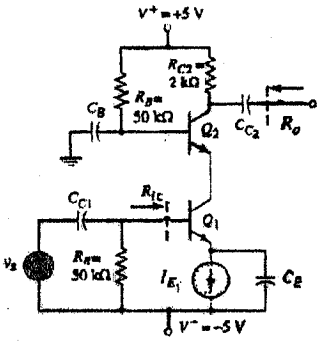

Fig. 2(c)

2. 選擇題(15 分)

Consider the circuits (a), (b), and (c) shown in Fig.2, assume that every transistor is biased in the forward-active mode and has the same $\beta_F = 100$, $V_{BE(on)} = 0.7$ V, and $V_A = \infty$. If the current sources I_{Co}, I_{Eo}, and I_{E1} are adjusted such that each Q_1 transistor has the same dc collector current and hence, the same small-signal parameters.

(1) Consider the voltage gain $A_v = v_o/v_i$, (A) $A_{va} > A_{vb} > A_{vc}$ (B) $A_{vb} > A_{vc} > A_{va}$ (C) $A_{va} = A_{vb} > A_{vc}$ (D) $A_{vb} > A_{va} > A_{vc}$ (E) $A_{vb} > A_{va} = A_{vc}$. (10 分，答錯倒扣 4 分)

(2) Consider the input resistance R_i, (A) $R_{ia} > R_{ib} > R_{ic}$ (B) $R_{ib} > R_{ic} > R_{ia}$ (C) $R_{ia} = R_{ib} > R_{ic}$ (D) $R_{ib} > R_{ia} > R_{ic}$ (E) $R_{ib} > R_{ia} = R_{ic}$. (5 分，答錯倒扣 2 分)

3. (20 分)

As shown in Fig. 3, assuming all transistors to be identical with β infinite, α = 1 and keeping the current in each junction the same.

(1) Derive an expression for the output current Io in terms of V_{CC}, V_{BE}, R_1, R_2 and R_E. (10 分)

(2) What will be the relationship of R_1, R_2 and R_E, which keeps output current Io independent of V_{BE}? (5 分)

(3) For V_{CC} =15 Volts, and V_{BE}=0.7 Volts, design the circuit to obtain an output current of 1 mA.

What is the lowest allowable voltage at the collector of Q_3? (5 分)

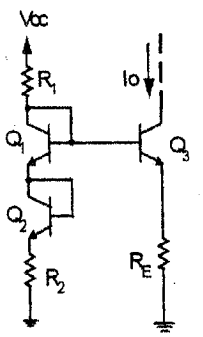

Fig. 3

注意：背面有試題

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4. (20 分)

For the amplifier as shown in Fig. 4, assuming that Vs has a zero dc component,

(1) Find the dc voltages V_{B1}, V_{B2}, V_{E2}, V_O and the dc emitter current I_{E2}. Let the BJTs have $\beta = 100$ and neglect I_{B2}. (10 分)

(2) Use feedback analysis to find the values of Vo/Vs and R_{in}. (10 分)

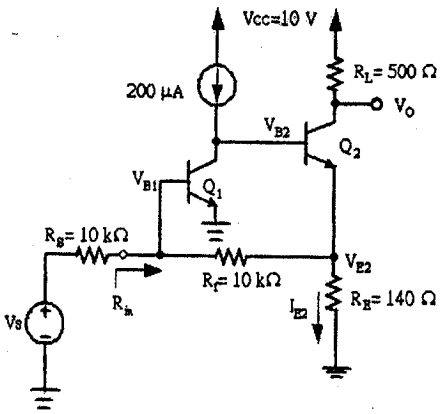

Fig. 4

5. (15 分)

In the shown circuit (Fig. 5), the internally compensated OP amp has high-order poles remote from its unity-gain frequency f_t, a relatively large open-loop gain A_O, and otherwise ideal characteristics.

(a) Find expression for the loop gain. (4 分)

(b) Find expressions for the potential conditions for oscillation. (8 分)

(c) Estimate the required value of R_2/R_1, if the angular frequency of oscillation is equal to $2/RC$. (3 分).

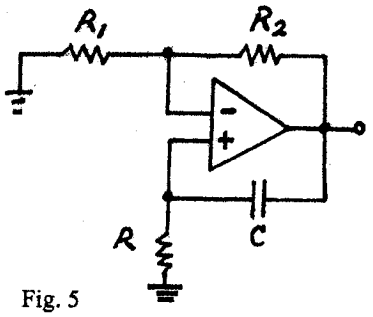

Fig. 5

6. (15 分)

For the shown one-transistor DRAM cell,

(a) if C_S = 20 fF, bit-line capacitance C_B = 1 pF, V_{DD} = 3.3 V, and NMOS transistor has a V_t (including the body effect) = 0.8 V, estimate the output readout voltage, i.e. change in the voltage on the bit line resulting from connecting a C_S to it, for a stored 1 and a stored 0, assuming the bit lines are precharged to $V_{DD}/2$ in a read operation. (10 分)

(b) if C_S = 15 fF, refresh is required within 5 ms, and a signal loss on the C_S of 0.3 V can be tolerated, estimate the largest acceptable leakage current present at the cell. (5 分)

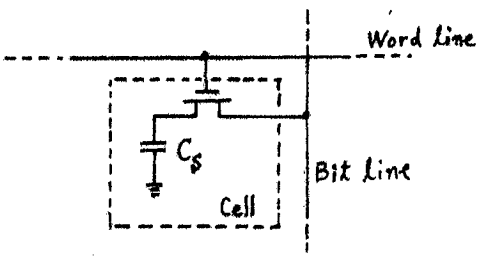

Fig. 6

參考用