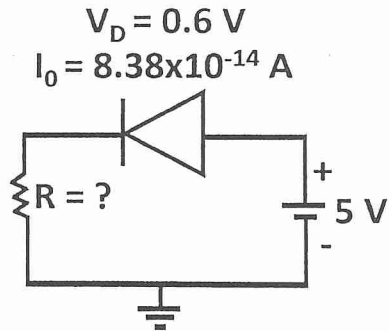


Choose the correct answer (25%):

- (1) In the circuit shown in the figure, what is the value of R if the diode voltage is $V_D = 0.6\text{ V}$ and the reverse-saturation current of the diode is $I_0 = 8.38 \times 10^{-14}\text{ A}$ and at room temperature ($T = 300\text{ K}$)?



- (A) 1 k Ω (B) 5 k Ω (C) 2 k Ω (D) 10 k Ω (E) 3 k Ω

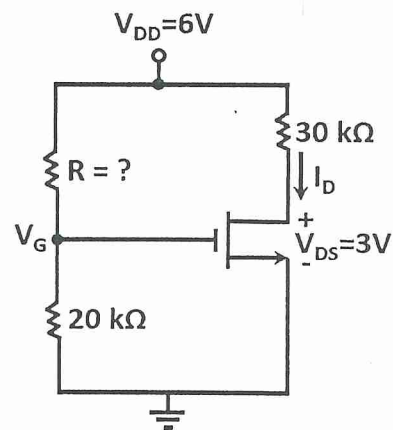
- (2) At $T = 300\text{ K}$, what is the built-in potential barrier of a Si pn junction with the doping concentration of $N_a = 2 \times 10^{16}\text{ cm}^{-3}$ in the p-region and $N_d = 5 \times 10^{16}\text{ cm}^{-3}$ in the n-region? (The intrinsic carrier concentration of Si is $n_i = 1.5 \times 10^{10}\text{ cm}^{-3}$)

- (A) 0.757 V (B) 0.601 V (C) 0.898 V (D) 0.562 V (E) 0.452 V

- (3) The threshold voltage of an n-channel enhancement-mode MOSFET is 0.5 V. If the conduction parameter of the MOSFET is $K_n = 1.4\text{ mA/V}^2$, what is the drain current (i_D) when the transistor is biased in the saturation region with the gate-to-source voltage (V_{GS}) of 1.6 V?

- (A) 2.02 mA (B) 0.22 mA (C) 1.69 mA (D) 1.21 mA (E) 0.66 mA

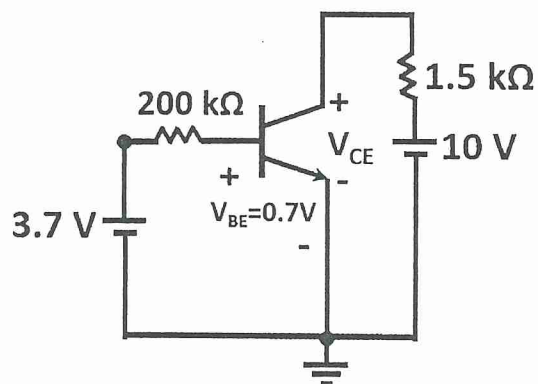
- (4) If the MOSFET shown in the figure is with the threshold voltage of 1 V and the conduction parameter (K_n) of 0.1 mA/V^2 , what is the value of R?



- (A) 20 k Ω (B) 10 k Ω (C) 50 k Ω (D) 30 k Ω (E) 40 k Ω

- (5) Using the parameters indicated in the circuit, determine the V_{CE} of the bipolar transistor with the dc common-emitter current gain of 200.

- (A) 5.5 V (B) 4 V (C) 3.5 V (D) 6.5 V (E) 3 V



參考用

注意：背面有試題

1. For the circuit shown in Fig. 1(a), the input and output voltages that are zero at $t = 0$ is driven by the input signal v_I shown in Fig. 1(b). The resistance and capacitance in the circuit are $R_1 = 5 \text{ K}\Omega$ and $C_2 = 0.2 \text{ }\mu\text{F}$. Determine the maximum value (5%) and minimum value (5%) of output signal v_O . Sketch and label the resulting output waveform v_O versus time (5%).

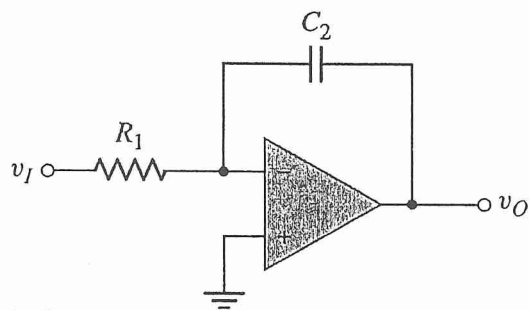


Fig. 1(a)

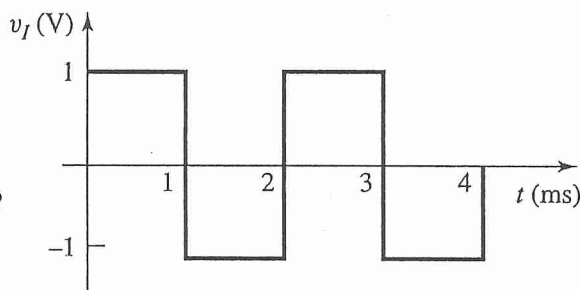


Fig. 1(b)

2. For the circuit shown in Fig. 2, assume transistor parameters of $V_{TN} = 0.5 \text{ V}$, $V_{TP} = -0.5 \text{ V}$, $K_n = 0.2 \text{ mA/V}^2$, $K_p = 0.1 \text{ mA/V}^2$, $\lambda_n = \lambda_p = 0.015 \text{ V}^{-1}$. Assume $V_{DD} = 5 \text{ V}$ and $I_{Bias} = 2 \text{ mA}$.
- Sketch the load line for transistor M_3 (5%).
 - Sketch the current-voltage characteristic for transistor M_2 (5%).
 - Determine the small-signal voltage gain $A_v = v_O/v_I$ (5%).

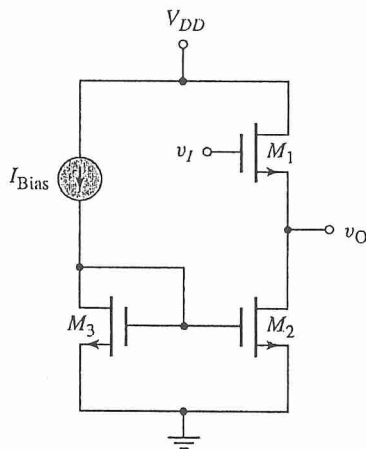


Fig. 2

3. For the circuit shown in Fig. 3, derive the expressions for the voltage transfer function $T(s) = V_o(s)/V_i(s)$ (5%), determine the cutoff frequency f_{3dB} (5%), and sketch Bode plots of magnitude (5%) and phase (5%) for the circuit.

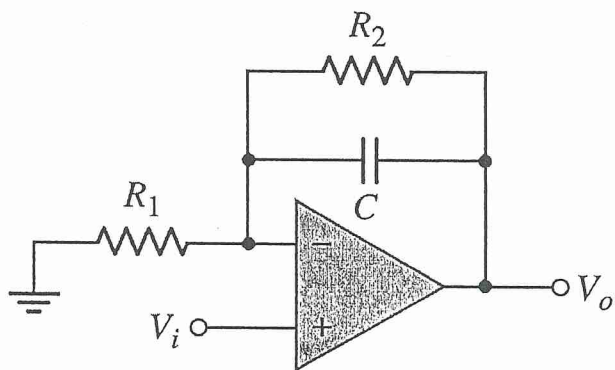


Fig. 3

參考用

注意：背面有試題

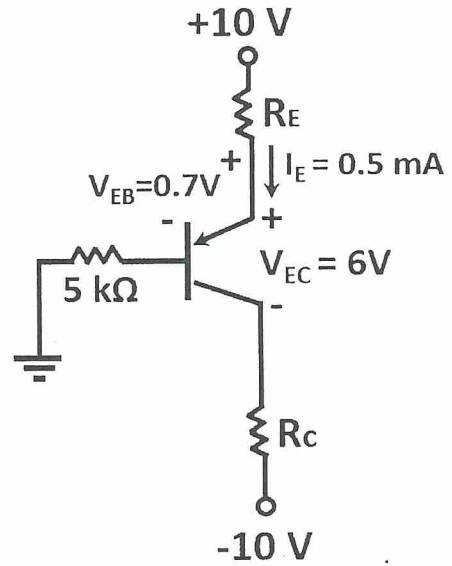
國立中央大學103學年度碩士班考試入學試題卷

所別：光電科學與工程學系碩士班 不分組(一般生) 科目：電子學 共 3 頁 第 3 頁

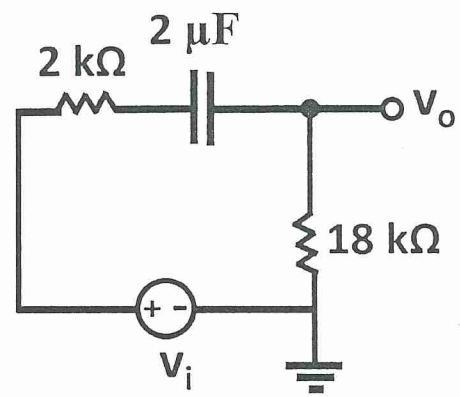
本科考試可使用計算器，廠牌、功能不拘

*請在試卷答案卷(卡)內作答

4. Assuming the dc current gain of the transistor shown in the circuit is $\beta = 99$, determine the values of R_E and R_C with the indicated parameters. (10 %)



5. Draw the Bode plot of the circuit with the indicated parameters. In the Bode plot, label the corner frequency and the maximum magnitude in dB. (15 %)



參考用