國立中央大學 113 學年度碩士班考試入學試題

所別： 光電類

科目： 電子學

＊本科考試可使用計算器，廠牌、功能不拘

本試題共四大題計算題，無計算過程不予計分。答案請標示單位。

1. (20%) A voltage amplifier with an input resistance R_i=5 kΩ and output resistance Ro=3 kΩ has an open-circuit voltage gain (A_{vo}) of 50 V/V (assuming frequency-independent). The amplifier is then capacitance-coupled to a 10 kΩ source and 1 kΩ load as shown in Fig.1.

   (a) (10%) What is the overall voltage gain ($\frac{v_o}{v_s}$) for DC and high frequency (f -> ∞)? Please describe the circuit as working as a low-pass, high-pass, or mid-pass filter.

   (b) (10%) What is the smallest C_1 and C_2 needed to make sure the cut-off frequency is less than 100 kHz? (You can separate input and output capacitors separately for a simple answer)

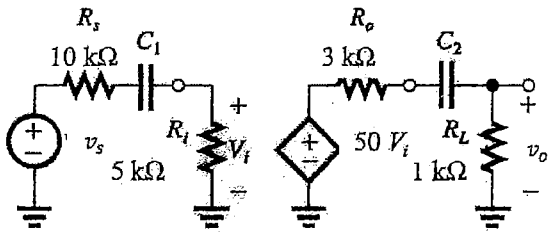

Figure 1

2. (30%) For the following BJT circuit in Fig. 2, two identical BJTs with β=100 are connected in cascade and used to amplify the signal. Please find the follows: (hints: you can assume V_{BE}=0.7V)

   (a) (12%) Determine the biasing current (I_{C1}, I_{C2}), base voltage (V_{B1}, V_{B2}), and collector voltage (V_{C1}, V_{C2}).

   (b) (18%) Find small-signal gain at 1st stage (v_{b2}/v_{sig}) and overall gain (v_o/v_{sig}).

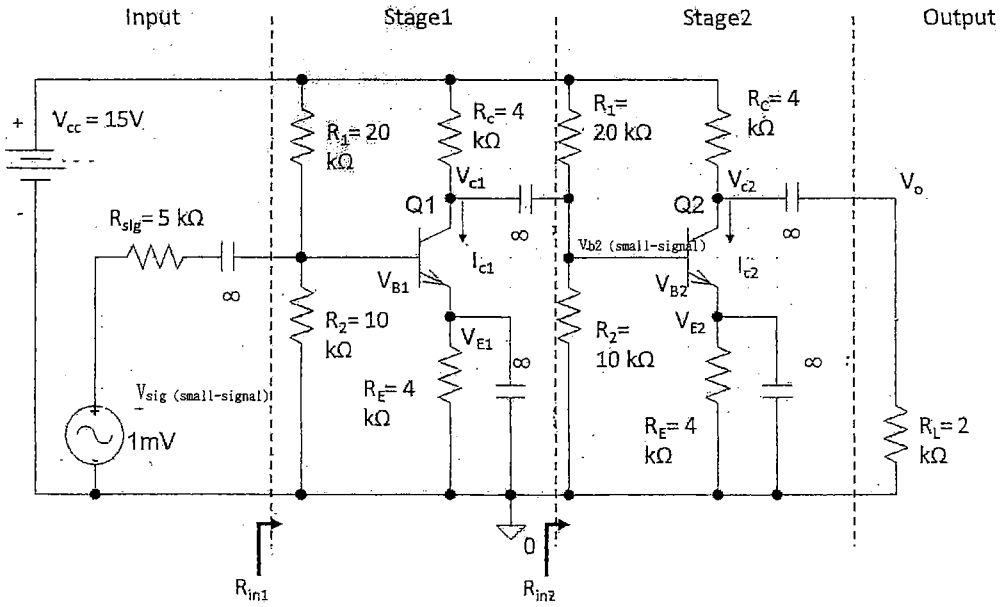

Figure 2

注意：背面有試題

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3. (20%) For the circuit in Figure 3, assuming OP amplifiers are ideal, please find the voltage of the correspond nodes, V_x, V_{out1}, V_{out2}, V_{out3}, and V_{out4}.

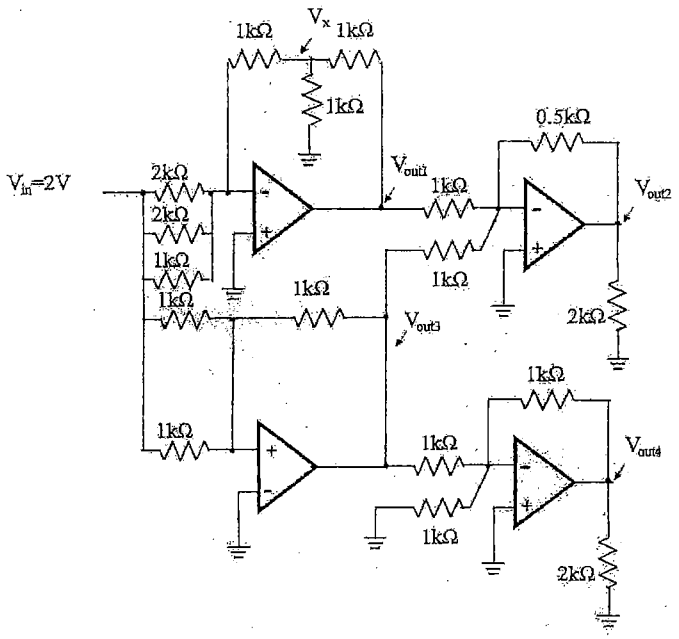

Figure 3

4. (30%) Refer the circuit shown in Fig. 4, a MOSFET differential pair is driven by a current source and connected with a variable resistance R_{SS} (200~800 kΩ). All MOSFETs are assumed to be the same with V_t=1V, $\mu_n C_{ox}$=1 mA/V^2 and W/L=40 for NMOS. Please evaluate the following:

(a) (10%) Please find the differential gain ($A_d=v_{od}/v_{id}$) if the MOSFETs are operated in the saturation regime. Hint: $v_{od}=v_{o2}-v_{o1}$

(b) (10%) If we apply the common-mode signal (v_{icm}) on both inputs. What is the minimal common-mode gain (v_{o1}/v_{icm}) at a single end by varying the R_{ss}?

(c) (10%) If the V_{min} required for the current sources is 0.5 V and both gate voltage at Q_1 and Q_2 are grounded. What is the restriction on V_{ss} for the operation regime of a differential amplifier?

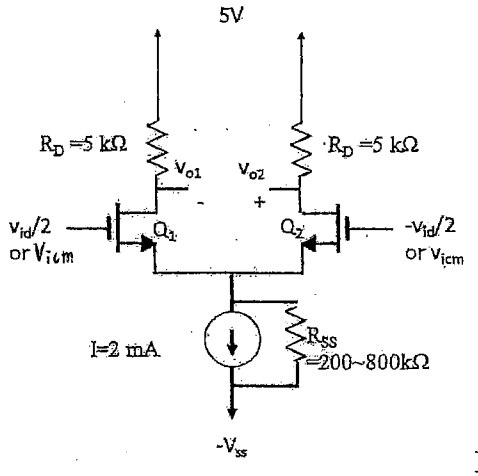

Figure 4

注意：背面有試題