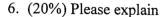
## 國立中央大學100學年度碩士班考試入學試題卷

所別:<u>通訊工程學系碩士班 乙組(通訊網路)(一般生)</u> 科目:<u>計算機系統</u> 共<u></u>頁 第<u>1</u>頁 本科考試禁用計算器 \*請在試卷答案卷(卡)內作答

- 1. (10%) Explain the following terms:
  - (1) (5%) Multiprotocol Label Switching (MPLS)
  - (2) (5%) Cloud Computing
- 2. (20%) Regarding to the IPv4 and IPv6 protocols,
  - (1) (10%) List and explain two technologies designed for prolonging the lifetime of IPv4.
  - (2) (10%) List and explain two technologies designed to integrate the IPv6 network into legacy IPv4 network.
- 3. (20%) The cyclic redundant check (CRC) mechanism has been widely employed to determine whether a received data frame is correct or not. What kinds of operations the following medium access control (MAC) protocols will perform when they detect an erroneous data frame.
  - (1) (10%) IEEE 802.3 (Ethernet)
  - (2) (10%) IEEE 802.11 (WiFi)
- 4. (20%) Consider a computer system with 512K (1K=2\*\*10) bytes cache memory and 32M (1M=2\*\*20) bytes main memory. Assume the set associative mapping is applied for cache management. The block size and set size of cache memory are 32 bytes and 256 bytes, respectively. Please,
  - (1) (10%) Show the mapping relation between cache memory and main memory.
  - (2) (10%) If the cache memory access time is 20 nanoseconds and main memory access time is 80 nanoseconds, what is the effective memory access time if the cache hit ratio is 0.75?
- 5. (10%) Consider a 5-stage (instruction fetch, instruction decode and register read/write, execution, memory, write back) pipeline, please explain how to overcome data hazard by using path forwarding for the following sample code? (please briefly indicate which stage to which stage of the forwarding path(s) is(are) designed for each required instruction).

Add 
$$r1, r2, r3$$
 /\*  $r2+r3 \rightarrow r1$   
Sub  $r4, r2, r1$  /\*  $r2-r1 \rightarrow r4$   
And  $r6, r3, r7$  /\* $r3(and)r7 \rightarrow r6$   
Or  $r2, r4, r7$  /\* $r4(or)r7 \rightarrow r2$ 



- (1) (5%) Dirty bit used for hierarchical memory management
- (2) (5%) Carry look ahead adder
- (3) (5%) Interrupt I/O v.s. DMA
- (4) (5%) Lower CPI means higher performance of system speed (true or false? and also provide your reason)

