國立中央大學九十六學年度電機系碩士在職專班招生試題

筆試科目：基礎電子學　　考試時間：100 分鐘　　共 1 頁，第 1 頁

1. 計算題與作圖題 (16 分)

Assuming an ideal op amp,

1-1 Find the transfer function of the circuit as shown in Fig. 1. (4 分)

1-2 What is the condition for which the output is independent of frequency? (3 分)

1-3 Letting $C_2 = 0.1\ C_1 = 0.1\ \mu F$ and $R_1 = 10\ k\Omega$, sketch Bode magnitude plots (in *rad/s*) for 3 cases: (9 分)

(a) $R_2 = 100\ k\Omega$; (b) $R_2 = 1\ M\Omega$; (c) $R_2 = 10\ k\Omega$.

2. 計算題 (10 分)

Figure 2 (a) and (b) shows the circuits using ideal diodes, find the values of the labeled voltages and currents. (10 分)

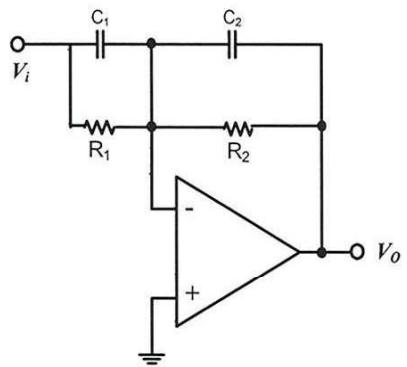

Fig. 1

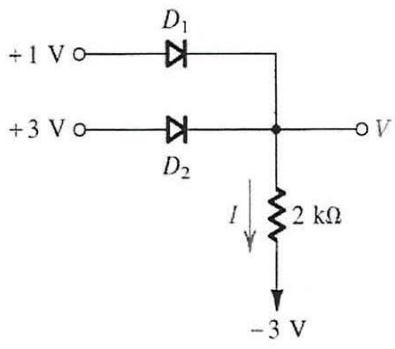

Fig. 2(a)

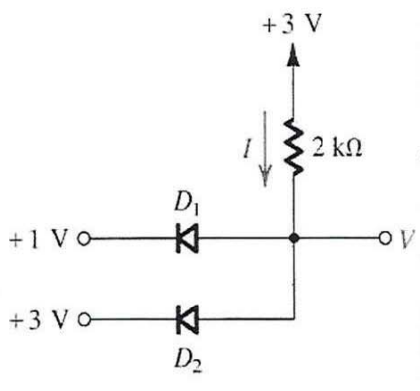

Fig. 2(b)

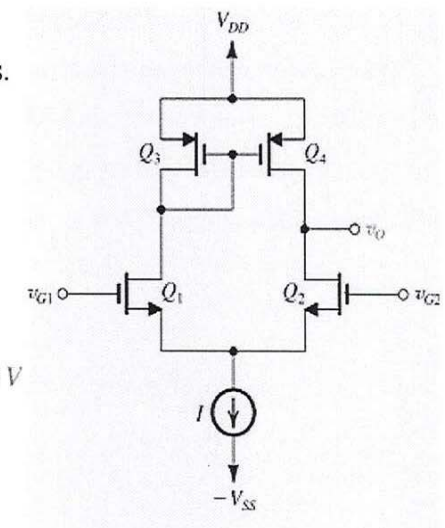

Fig. 3

3. 計算題 (20 分)

Figure 3 shows a CMOS differential amplifier with active load, the design parameters of this amplifier are listed as follows: $(W/L)_n = 100$, $(W/L)_p = 200$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 0.2\ mA/V^2$, $V_{An} = |V_{Ap}| = 20\ V$, $I = 0.8\ mA$, $R_{SS} = 25\ k\Omega$，where R_{SS} is the equivalent output resistance of current source I; Please find (a) overall transconductance G_m, (5 分) (b) output resistance R_O, (5 分) (c) differential gain A_d, (5 分) and (d) common mode rejection ratio (CMRR). (5 分)

4. 計算題 (20 分)

Figure 4(a) shows a BJT circuit with $V_{CC} = 10\ V$, $I = 1\ mA$, $\beta = 100$, $R_B = 100\ k\Omega$, and $R_C = 7.5\ k\Omega$;

4-1 Find the dc voltage at the base, emitter, and collector, assuming $V_{BE} = 0.7\ V$. (4/3/3 分)

4-2 For $V_{EE} = 10\ V$, find the required value of R for the circuit of Fig. 4(b) in order to realize the current source I. (10 分)

5. 問答題與計算題 (18 分)

The voltage-transfer characteristic of a particular logic inverter is observed to have the following salient features: The upper output voltage level is 1.8 V; The lower output voltage level is 0 V; The slope of the characteristic is -1 V/V for inputs of 0.98 V and 0.65 V; The maximum slope is about -40 V/V occurring where the input and output voltages each equal 0.82 V.

5-1 Sketch and label the transfer characteristic. (4 分)

5-2 Find values for $V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th}(= V_M)$, NM_L, and NM_H. (14 分)

6. 問答題與計算題 (16 分)

6-1. A particular 1 Mb DRAM uses a square cell array with 4-bit readout.

(a) How large a word-line (row) decoder is needed? (4 分)

(b) How large a bit-line (column) decoder is needed? (4 分)

(c) For a 1024-row decoder, how many address bits are used? (4 分)

6-2. In a particular DRAM technology, cell leakage currents can be reduced to 1 fA. What is the minimum allowable capacitor for 10 ms refresh interval with a recoverable cell-voltage loss of 0.5 V? (4 分)

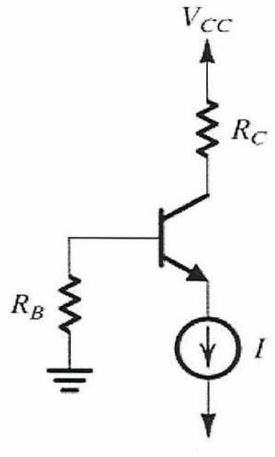

Fig. 4 (a)

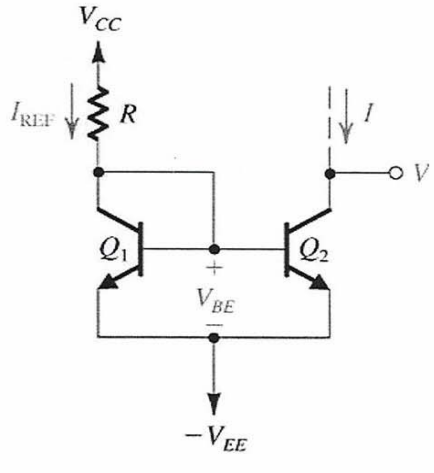

Fig. 4 (b)