國立中央大學102學年度碩士班考試入學試題卷

所別：電機工程學系碩士班 固態組(一般生)　科目：電子學　共 2 頁　第 1 頁
電機工程學系碩士班 電波組(一般生)
電機工程學系碩士班 系統與生醫組(一般生)

本科考試禁用計算器

＊請在試卷答案卷（卡）內作答

參考用

1. 計算題 (10 分)

Fig. P1 shows a signal source V_s connected to the input of an amplifier. Here R_s is the signal source resistance, R_i and C_i are the input resistance and input capacitance of the amplifier, respectively.

1-1 (5 分) Using R_s, R_i and C_i derive an expression for $V_o(s)/V_s(s)$.

1-2 (5 分) Find the 3-dB frequency for the case R_s = 24 kΩ, R_i = 120 kΩ, and C_i = 5 pF.

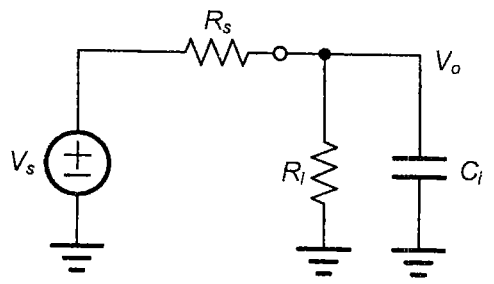

Fig. P1

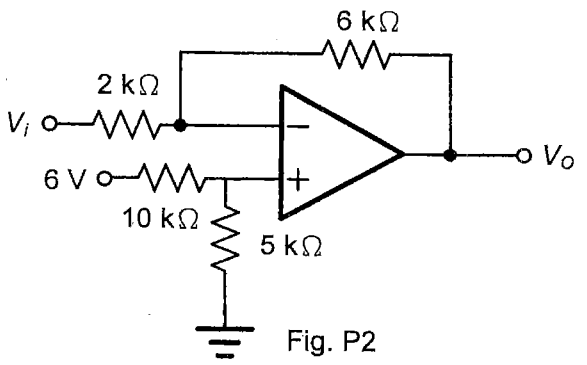

Fig. P2

2. 計算題 (10 分)

Assuming ideal op amplifier as shown in Fig. P2,

2-1 (5 分) Find the expression for the output voltage V_o as function of V_i , *i.e.*, $V_o = f(V_i)$.

2-2 (5 分) Find the Input resistance of the circuit.

3. 計算題 (15 分；每子題 3 分)

The node voltage data in the following table apply to an NMOS transistor with a threshold voltage V_{tn} = 0.4 V. V_G is the gate voltage, and $V_{S/D}$ in the blank is the source voltage or drain voltage. Neglect the body effect, determine the cases (a) ~ (e) are operated in the saturation region, triode region or cutoff region.

	$V_{S/D}$	V_G	$V_{S/D}$
(a)	0.4	2.2	1.5
(b)	2.4	2.6	1.8
(c)	-0.4	-1.2	-2.5
(d)	3.9	4.2	4.5
(e)	3.4	1.2	0.5

4. 計算題(15 分；每子題 5 分)

Fig. P4 shows a particular configuration of MOS amplifiers, known as "source follower." The body voltage of the MOS M_1 and M_2, $V_{b1} = V_{b2} = 0$ V are not shown in the figure.

4-1 Consider the body effect, replace the MOS transistors $M_1$and M_2 with theirs small signal model g_m, g_{mb} and r_o.

4-2 Find the output resistance r_o .

4-3 Find the voltage gain v_{out}/v_{in}.

5. 計算題(15 分；每子題 5 分)

Fig. P5 shows a Darlington voltage follower which is operated with I_{E2} = 5 mA, R_E = 1 kΩ, R_{sig} = 100 kΩ, and $\beta_1 = \beta_2$ =100.

5-1 Find the input resistance R_{in}.

5-2 Find the output resistance R_{out}.

5-3 Find the voltage gain v_o/v_{sig}.

注意：背面有試題

所別：電機工程學系碩士班 固態組(一般生)　科目：電子學　共 2 頁 第 2 頁
電機工程學系碩士班 電波組(一般生)
電機工程學系碩士班 系統與生醫組(一般生)
本科考試禁用計算器

＊請在試卷答案卷（卡）內作答

參考用

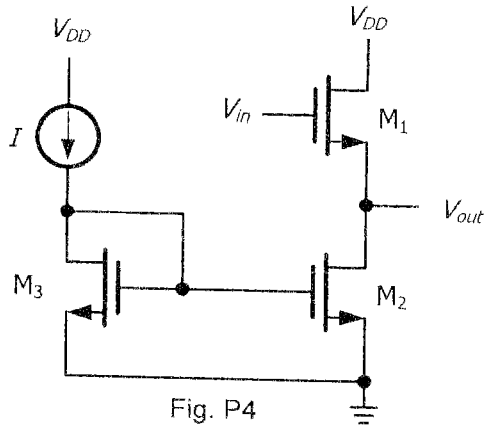

Fig. P4

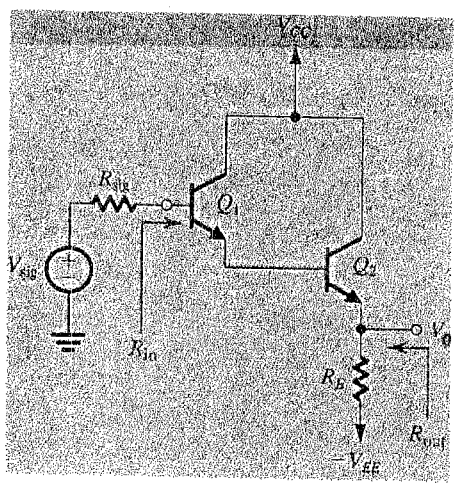

Fig. P5

6. 選擇題與計算題(15 分)

Fig. P6 shows a feedback circuit, which consists of a common gate amplifier formed by Q_1 and R_D. The capacitive divider C_1, C_2 senses the output voltage, applying the result to the gate of common source transistor Q_f. The bias circuit for Q_f is not shown. The design parameters are illustrated as follows, g_{m1} = 5 mA/V, g_{mf} = 1 mA/V, R_D = 10 kΩ, C_1 = 0.9 pF, and C_2 = 0.1 pF. Assume that C_1 and C_2 are sufficiently small that their loading effect on the basic amplifier can be neglected. Also neglect output resistance r_o and body effect.

6-1 (5 分) Identify the feedback topology to be used. (A) shunt-series, (B) series-series, (C) shunt-shunt, (D) series-shunt.

6-2 (10 分) Set I_s = 0 and find the loop gain by breaking the loop at the gate termination of transistor Q_f.

7. 計算題(15 分; 每子題 5 分)

Fig. P7 shows a cascade connection of a low pass filter and a high pass filter using an ideal unity-gain buffer amplifier. This circuit gives a band pass filter response. The transfer function of the band pass filter can be written as below, where a_1, ω_0, and Q are the center frequency gain, center frequency and quality factor, respectively. Please derive a_1, ω_0, and Q in terms of R, C, and k.

$$T(s)=\frac{V_o(s)}{V_i(s)}=\frac{a_1 s}{s^2+(\frac{\omega_0}{Q})s+\omega_0^2}$$

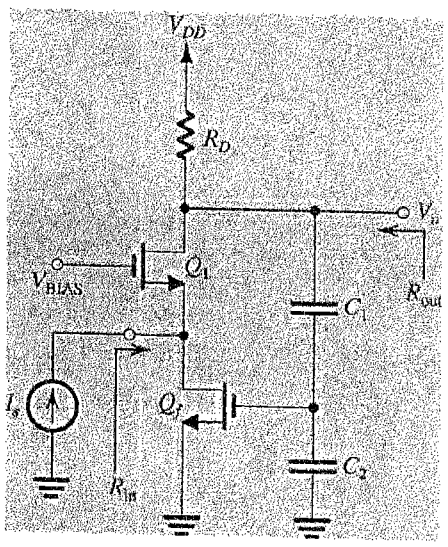

Fig. P6

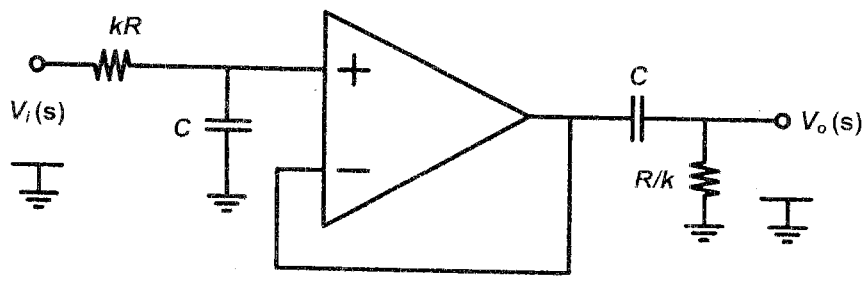

Fig. P7

8. 計算題(5 分)

Sketch a CMOS logic-gate circuit realization for the function $Y=\overline{A+B(C+D)}$.

注意：背面有試題