////////////////////////　請依順序作答　////////////////////////

1. (20%)

(a) (7%) If A=39_{10}, B= -49_{10}. Express A, B and A+B by using 7-bit 2's complement number system. The procedure of operation shall be written down.

(b) (3%) Express A in 8-bit odd-parity code.

(c) (5%) Define a 4-bit code for representing 0,1,2,...,9. The code words have the property that for any two *consecutive digits* (digits whose difference is 1), they differ in only one bit position. This property also holds for the digits 0 and 9.

(d) (5%) Using switching algebra to simplify $f = ab+a'c+bc$. The procedure of simplification shall be written down.

2. (20%) ($A_4A_3A_2A_1$) denotes a BCD (binary coded decimal) code as shown in Table 2。The output of the system *(f)* is logic 1 only if the ($A_4A_3A_2A_1$) is greater than or equal to 5. Otherwise, the output is logic 0。

(a) (3%) Write down the truth table of the system *f*。

(b) (4%) Using K-map to express f in minimum sum-of-product form。

(c) (5%) Design *f* using only 2 and 3 inputs NAND gates. Remember that the inputs are A_4, A_3, A_2, A_1. If you need the complements of A_4, A_3, A_2, A_1, you need to generate them in your design. Draw its logic diagram。

(d) (8%) Explain: What is static hazards? Does the design in Problem 2(c) has such problem? If the answer is yes, how to improve it?

Table 2 BCD code

0:	0000	5:	0101
1:	0001	6:	0110
2:	0010	7:	0111
3:	0011	8:	1000
4:	0100	9:	1001

3. (20%)

(A) (5%) Find the minimum sum-of-product (SOP) and the minimum product-of-sums (POS) expression for the logic function

$$f(A,B,C,D) = A'B' + B'C' + A'BD' + AC'D + A'BD + AB'CD'$$

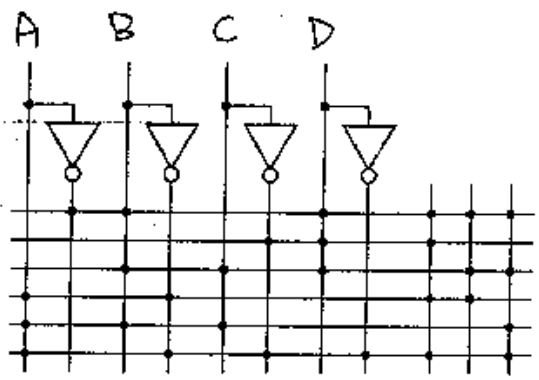
Show your K-map and derivation in your answer sheet.

(B) (15%) The internal connection diagram for a PLA is given in Fig. 3.

(i) (3%) Write down the output logic functions, X, Y, Z, that are realized in the PLA. You don't have to simplify those logic functions.

(ii) (6%) Try to realize the logic function of Y using (a) (2%) a 16-to-1 multiplexer (b) (4%) an 8-to-1 multiplexer.

(iii) (6%) Try to realize the logic function of Z using (a) (3%) an active-low output 16-to-1 decoder plus one 4-input basic gate (AND/OR/NAND/NOR gate) (b) (3%) an active-high output 16-to-1 decoder plus one 4-input basic gate (AND/OR/NAND/NOR gate).



(Fig.3)

4. (22%) Analyze the circuit shown in Fig. 4(a). The circuit contains two clocked negative edge-triggered JK flip-flops. The binary input and output are *x*, *z*, respectively. The outputs of the two JK flip-flops are y1 and y2.
   (i) (12%) Fig. 4(b) shows the input waveform of x signal and the input clock. Please plot the waveforms of y1, y2 and, z signals. That is, show the timing diagram of the circuit. Note that at time 0, the initial states of JK flip-flops are y1=y2=1.
   (ii) (10%) If we encode y1 and y2 as state A, B, C, and D as shown in Fig. 4(c). Try to show the (a) State table (b) State diagram of the sequential circuit.

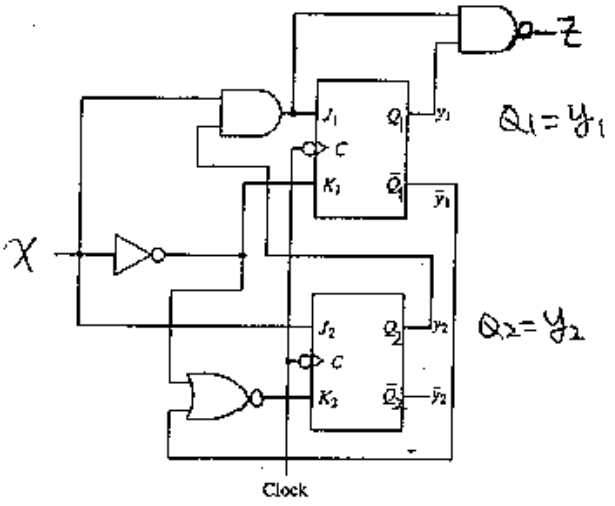


Fig. 4(a)

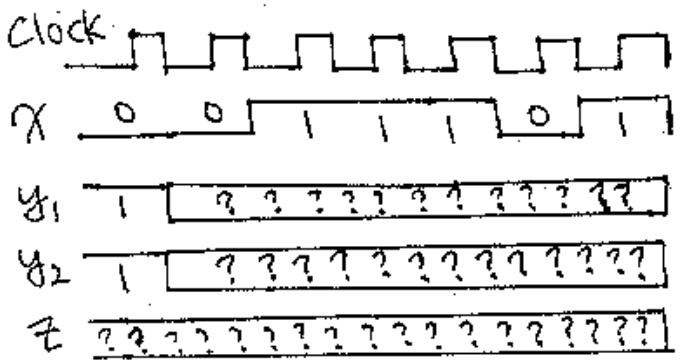


Fig. 4(b)

y_1	y_2	State Assignment
0	0	A
0	1	B
1	1	C
1	0	D

Fig. 4(c)

5. (18%) A Moore sequential circuit has one input, X, and one output Z. When the input sequence 011 occurs, the output becomes 1 and remains 1 until the sequence 011 occurs again in which case the output returns to 0. The output then remains 0 until 011 occurs a third time, *etc.* For example, the input sequence

   X = 0 1 1 0 1 0 1 1 0 1 0 0 1 1, has the output

   Z = 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 1 1

   Please derive the (a) State table (b) State diagram of the sequential circuit. Use minimum number of states.