所別：電機工程學系碩士班 甲組(一般生) 科目：電子學

(學位在職生)

1. 計算題 (20 分)

1-1 (5 分) The circuit of Fig. 1(a) is a source follower configuration with positive feedback. The transconductances of $Q_1$ and $Q_2$ are $g_{m1}$ and $g_{m2}$, respectively. The capacitances $C_{gs}$ and $C_{gd}$ can be neglected. Also neglect output resistance $r_O$ and body effect. Calculate the input resistance $R_{in}$.

1-2 (5 分) The circuit of Fig. 1(b) is a common-source with a resistive feedback which can be used as a lossy active inductor. Calculate the s-domain output resistance $Z_{out}(s)$ in terms of $R_F$, $g_m$, $C_{gs}$, and $C_{gd}$.

1-3 (10 分) The circuit of Fig. 1(c) is a gyrator which can be used as an active inductor. Assume that ideal op amps are applied in the circuit. Calculate the s-domain input impedance $Z_{in}(s)$.

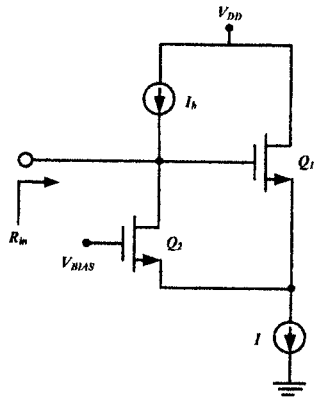


Fig. 1(a)

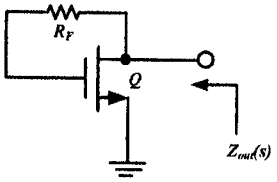


Fig. 1(b)

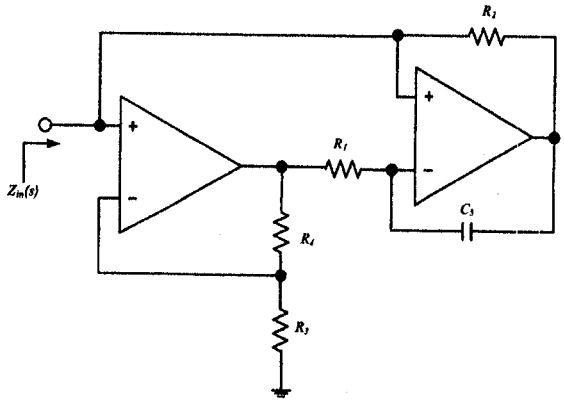


Fig. 1(c)

2. 計算題 (15 分)

A feedback circuit is shown in Fig. 2, which consists of a common-gate amplifier formed by $Q_1$ and $R_D$. The capacitive divider $C_1$, $C_2$ senses the output voltage, applying the result to the gate of common-source transistor $Q_f$. The bias circuit for $Q_f$ is not shown. The design parameters are illustrated as follows, $g_{m1} = 5$ mA/V, $g_{mf} = 1$ mA/V, $R_D = 10$ kΩ, $C_1 = 0.9$ pF, and $C_2 = 0.1$ pF. Assume that $C_1$ and $C_2$ are sufficiently small that their loading effect on the basic amplifier can be neglected. Also neglect output resistance $r_O$ and body effect.

2-1 (10 分) Derive the expressions of the transimpedance gain $V_O / I_S$.

2-2 (5 分) Find the output resistance $R_{out}$.

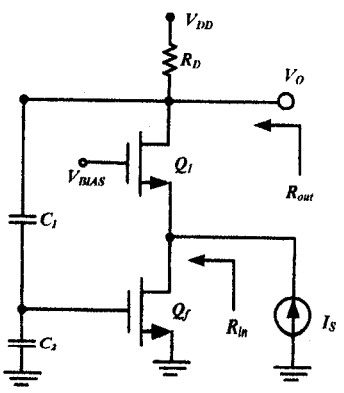


Fig. 2 Circuit for Problem 2

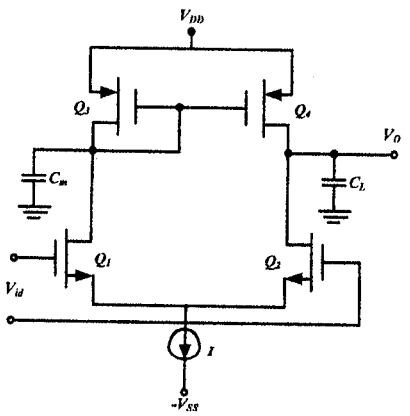


Fig. 3 Circuit for Problem 3

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3. 計算題 (15 分)

A CMOS active-loaded differential amplifier is shown in Fig. 3. For this process, assume that for all transistors $W/L$=5.0 μm/0.25 μm. The design parameters are listed as follows: $\mu_n C_{ox}$ = 250 μA/V$^2$, $\mu_p C_{ox}$ = 100 μA/V$^2$, $V'_{An}$=5 V/μm, and $|V'_{Ap}|$ = 6 V/μm. The bias current $I$ = 0.2 mA, and bias current source has an output resistance $R_{SS}$ = 25 kΩ and an output capacitance $C_{SS}$ = 0.2 pF. And the total capacitance at the input of the current mirror is $C_m$=50 fF. The total capacitance at the output is $C_L$= 40 fF.

3-1 ( 6 分) Calculate the low frequency values of differential gain $A_d$, and common mode gain $A_{cm}$.

3-2 ( 6 分) Derive the expressions of the high frequency differential gain $A_d(s)= V_O / V_{id}$ in terms of $g_{m1}$, $g_{m3}$, $C_L$, $C_m$, $R_O$ ($R_O$ is the resistance of $r_{02}$ and $r_{04}$ in parallel).

3-3 (3 分) The value of dominant pole $f_{p1}$.

4. 電路設計題:Static CMOS (15 分)

Design the static complementary MOS pullup and pulldown networks for these logic expressions:

4-1 ( 5 分) F1 = (AB+CD)'

4-2 ( 5 分) F2 = [(A+B)C+D]'

4-3 ( 5 分) For a CMOS process, assume that the mobility for MOS transistors $\mu_n$ = 3 $\mu_p$, $|V_{tp}| = V_{tn}$, and the minimum channel lengths for all MOS transistors are chosen. Size the width of MOS transistors in problem 4-1 such that the circuit's rise and fall times are approximately equal.

5. 電路設計題:Pseudo-nMOS and dynamic CMOS gates (10 分)

Design the circuits for pseudo-nMOS gate and dynamic CMOS gate for the function F = [( A+B+C)D+ EF ]'

6. 電路設計題:Dynamic shift register (10 分)

Memory is an important part of digital systems. It is for temporary storage of the output produced by a combinational circuit for use at a later time in the operation. The simplest memory machine we can build with the dynamic latch is a shift register. Design a one-bit input and a one-bit output positive edge-triggered dynamic Master-slave D-type shift register. The circuits you need are two inverters and two CMOS transmission gates.

7. 簡答與說明題(15 分)

7-1 (5 分) Derive the expressions of the dynamic switching power of CMOS logic circuit. Can we reduce the power by decrease the operation frequency?

7-2 (5 分) Find the output function of Fig.7-2.

7-3 (5 分) Find the output function $C_3$ of Fig.7-3.

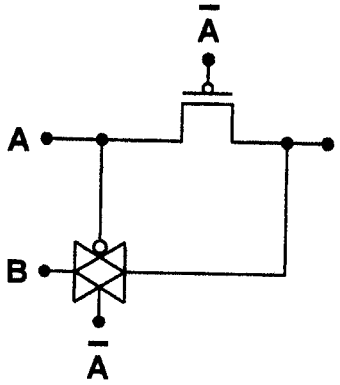


Fig. 7-2 Circuit for Problem 7-2