

國立中央大學104學年度碩士班考試入學試題

類別：資工類

科目：作業系統與計算機組織 共 5 頁 第 1 頁

\*請在答案卷(卡)內作答

本科考試禁用計算器

參考用

單選題 (共 20 分)

1. (4 pts.) The information of a virtual memory system is assumed to be:

- Page size: 1024 words
- Number of virtual pages: 8
- Number of physical pages: 4
- The current page table is

VPN	0	1	2	3	4	5	6	7
PPN	2	1	NULL	NULL	3	NULL	0	NULL

For the following (decimal) virtual word addresses: VA1: 57, VA2: 2048, VA3: 1026, VA4: 7749, VA5: 6150, their corresponding physical addresses are PA1, PA2, PA3, PA4, PA5.  $K = (PA1 + PA2 + PA3 + PA4 + PA5) \bmod 5$ , where "mod" is the modulo operator, and PA=-1 if it is a page fault. What is "K"?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4.

2. (4 pts.) A cache with data size 1Mbytes contains 32768 blocks and is eight-way set associative. The byte address 0x11D9A4F1 is accessed and is a hit in this cache. Assume that the corresponding tag value is "T", what is "T mod 5"?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4.

3. (4 pts.) Given a function or output F with four inputs: A,B,C,D as  $F(A,B,C,D) = \sum(3,4,5,6,7)$  (minterms)

and its don't care information is  $d(A,B,C,D) = \sum(10,11,14,15)$ . By the commonly used Karnaugh Map, simplify F with the minimum number of gates using "product of sum" and there are "M" OR gates, "N" AND gates, "P" NOT/INVERT gates, where each AND/OR gate has two inputs and NOT gate has one input.  $K = (M \times 4 + N \times 3 + P) \bmod 5$ . What is "K"?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4.

4. (4 pts.) "M" is a floating-point number in the format of IEEE754 single precision:

0100000001010101010101010101010

$K = \{\text{Round}(M \times 20)\} \bmod 5$ . What is K?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4.

5. (4 pts.) There are three classes of instructions: Class A, Class B and Class C. The CPI values for Classes A, B and C are 3, 2 and 1 respectively. We have two compilers, C1 and C2. The compiler C1 generates  $10^6$  Class A instructions,  $2 \times 10^6$  Class B instructions and  $5 \times 10^6$  Class C instructions. The compiler C2 generates  $10^6$  Class A instructions,  $10^6$  Class B instructions and  $10^7$  Class C instructions. If C1 is tested on a 1GHz machine, M1, while C2 is tested on a 1.5GHz machine, M2, the execution time of {C1,M1} is "T1" ms (milliseconds) while the execution time of {C2,M2} is "T2" (milliseconds). Calculate

注意：背面有試題

本科考試禁用計算器

$$K = \{\text{Round}(|T1 - T2| \times 1234)\} \bmod 5.$$

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4.

參考用

多選題(每題 5 分，共 80 分，答錯每選項倒扣 1 分)

6. (5 pts.) Which of the following statements are true:
- (A) Page table is a cache.
  - (B) TLB is a cache.
  - (C) "TLB miss, Page table hit, Cache miss" is possible.
  - (D) Conflict misses only occur in a direct-mapped or set -associative cache and can be eliminated in a fully associative cache of the same size.
  - (E) A very large cache can avoid all the misses.
7. (5pts.) Which are the causes that limit the growth of uniprocessor performance and motive the trend of developing multiple processors per chip in recent years?
- (A) Long memory latency
  - (B) Emergence of Reduced Instruction Set Computer
  - (C) Limits of power
  - (D) Little instruction-level parallelism left to exploit efficiently
  - (E) None of the above
8. (5 pts.) Suppose that the frequency of Floating Point (FP) operations is 25% and the average Clock Cycle Per Instruction (CPI) of FP operations is 4. The frequency of Floating Point Square Root (FPSQR) operations is 2% and the average Clock Cycle Per Instruction (CPI) of FP operations is 20. The average CPI of other instructions is 1.33. There are two alternatives to improve the processor. Alternative 1 is to reduce the CPI of FPSQR to 2. Alternative 2 is to reduce the average CPI of all FP to 2. Which of the following is true?
- (A) Alternative 1 is better.
  - (B) Alternative 2 is better.
  - (C) The CPI of alternative 1 is 1.25.
  - (D) The CPI of alternative 2 is 1.25.
  - (E) The speedup for alternative 2 is 1.33.
9. (5 pts.) Which of the following statements are true for General-purpose register (GPR) instruction architecture?
- (A) One of the advantages of register-register instructions is simpler code-generation
  - (B) The instruction count for register-register instructions is usually lower than register-memory instructions.
  - (C) Using registers is more efficient for a compiler than other forms of internal storage.
  - (D) When variables are allocated to registers, the memory traffic reduces, the program speeds up.

注意：背面有試題

本科考試禁用計算器

(E) None of the above

10. (5 pts.) About single -cycle implementation and multi-cycle implementation of control and data path, which of the following statements are true?

- (A) Single -cycle implementation of control and data path is better than multi-cycle implementation.
- (B) Multi-cycle implementation of control and data path prevents an instruction from sharing functional units with another instruction within the execution of the instruction.
- (C) Single -cycle implementation facilitates the design of pipeline.
- (D) For multi-cycle implementation, the clock cycle is determined by the longest possible path.
- (E) None of the above.

11. (5 pts.) Considering the following code sequence.

```

1  Loop: LD  F0,0(R1)
2          SUBI R1, R1, 8
3          ADDD  F4, F0, F2
4          stall
5          BNEZ  R1, Loop
6          SD  8(R1), F4

```

Unroll four times and rearrange the code to minimize the stalls

```

1  Loop: LD  F0,0(R1)
2  LD  F6, -8(R1)
3  LD  F10, -16(R1)
4  LD  F14, -24(R1)
5  ADDD  F4, F0, F2
6  ADDD  F8, F6, F2
7  ADDD  F12, F10, F2
8  ADDD  F16, F14, F2
9  SD  0(R1),F4
10 SD  -8(R1),F8
11 SUBI R1, R1, #32
12 SD  A(R1), F12
13 BNEZ  R1, LOOP
14 SD  B(R1), F16

```

Where **A** and **B** stand for two numbers. Which of the following is true.

- (A) Number **A** in line 12 should be 8. (B) Number **A** in line 12 should be 16.
- (C) Number **B** in line 14 should be 8. (D) Number **B** in line 14 should be 16.
- (E) Number **B** in line 14 should be 32.

參考用

注意：背面有試題

12. (5 pts.) Which of the following instructions should be privileged?

- (A) Set value of timer. (B) Read the clock. (C) Clear memory.  
(D) Issue a trap instruction. (E) Turn off interrupts.

13. (5 pts.) Identify the following environments need hard real-time scheduling.

- (A) Thermostat in a household. (B) Control system for a nuclear power plant.  
(C) Fuel economy system in an automobile. (D) Landing system in a jet airliner.  
(E) Mailing system.

14. (5 pts.) Consider the following code segment:

```
pid_t pid;
pid = fork();
if (pid == 0) { /* child process */
    fork();
    thread_create(...);
}
```

參考用

fork();

- a. How many unique processes are created? and  
b. How many unique threads are created?

Please select the correct answer:

- (A) two processes (B) four processes (C) six processes (D) two threads (E) four threads

15. (5 pts.) Consider the following segment table:

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

What are the physical addresses reference in the following item will cause an illegal address trap to OS for the following logical addresses?

- (A) 0,430 (B) 1,10 (C) 2,500 (D) 3,400 (E) 4,112

16. (5 pts.) Which of the following scheduling algorithms could result in starvation?

- (A) First-come, first-served (B) Shortest job first (C) Round robin (D) Priority (E) None

17. (5 pts.) Choose the correct statements from the multiple choices regarding DMA.

- (A) DMA is a mechanism for allowing an I/O device to transfer data to and from memory without involving the CPU in the transfer.
- (B) In DMA only one interrupt is generated per byte.
- (C) While the DMA controller is performing the data transfer, the CPU is free to perform other tasks.
- (D) The cycle stealing in DMA can speed up the CPU computation.
- (E) DMA can perform a transfer between two memory-mapped devices without the intervention of the CPU or the use of main memory.

18. (5 pts.) Choose the correct statements from the multiple choices regarding context switch.

- (A) A context switch from one process to another can be accomplished without executing OS code in kernel mode.
- (B) Paging increases the context-switch time.
- (C) Network traffic can cause a high context-switch rate.
- (D) The smaller the time quantum in RR scheduling, the more context switches.
- (E) None of the above.

19. (5 pts.) Choose the correct statements from the multiple choices regarding deadlock.

- (A) Deadlock prevention requires that the operating system is given in advance additional information concerning which resources a process will request and use during its lifetime.
- (B) If a resource-allocation graph has a cycle, the system is in a deadlock state.
- (C) An unsafe state means the system is in deadlock.
- (D) Deadlock can never occur if no process is allowed to hold a resource while requesting another resource.
- (E) To deal with deadlocks, most operating systems, including UNIX, pretend that deadlocks never occur in the system.

20. (5 pts.) Choose the correct statements from the multiple choices regarding policies and mechanisms.

- (A) Policies decide how to do something.
- (B) Policies are likely to change from place to place or time to time.
- (C) "How long the timer for CPU protection is set for a particular user" is a mechanism.
- (D) "What the punishments are if the procedures are not followed" is a policy decision.
- (E) Firewall is a mechanism for access restriction.

21. (5 pts.) Choose the correct statements from the multiple choices regarding ICMP and OSPF.

- (A) The traceroute command can be implemented by ICMP messages.
- (B) The ping utility can be implemented by ICMP messages
- (C) OSPF is based on Dijkstra's algorithm.
- (D) OSPF is a kind of distance-vector routing protocols.
- (E) OSPF is a kind of exterior gateway protocols.

參考用