國立中央大學 105 學年度碩士班考試入學試題

所別： 資工類　　共 7 頁　第 1 頁

科目： 作業系統與計算機組織

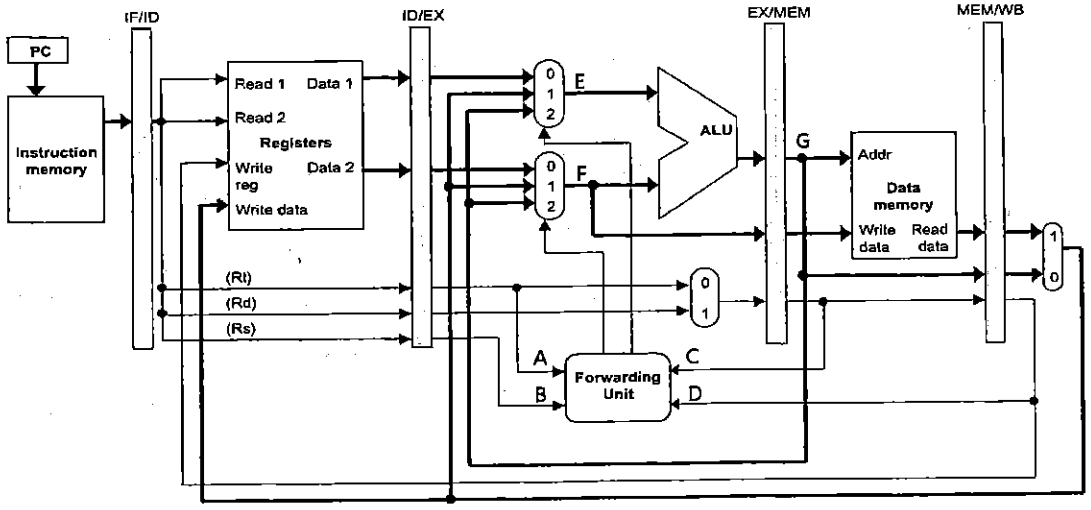
本科考試禁用計算器　　＊請在答案卷(卡)內作答

單選題（答錯倒扣 2 分）

1. (4 pts.) Use 32-bit IEEE 754 single precision to encode "-1234.6875". If K is the number of "1" in this 32-bit value, then what is "K mod 5"?
   (A) 0 (B) 1 (C) 2 (D) 3 (E) 4

2. (4 pts.) Assume that the number of data dependencies existing in the following MIPS code segment is K. What is "K mode 5"?
   (A) 0 (B) 1 (C) 2 (D) 3 (E) 4
   add $6, $4, $5
   add $2, $5, $6
   sub $3, $6, $4
   add $2, $2, $3

3. (4 pts.) Following the previous question. Assume that the code will be processed by the pipelined datapath shown below and assume that the registers initially contain their number plus 100. For example, $2 contains 102 and $5 contains 105, etc. In the fifth clock, calculate the sum of A, B, C, D, E, F and G. If this sum is equal to K, what is "{Round(K/3)} mod 5"?
   (A) 0 (B) 1 (C) 2 (D)3 (E) 4



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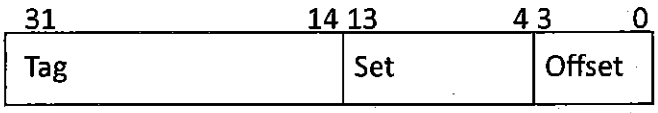
4. (4 pts.) A system has a 256 Kbyte cache memory and the address format is



The cache should be (A) 2-way set associative (B) 4-way set associative (C) 8-way set associative (D) a direct mapped cache (E) None of above.

5. (4 pts.) In a 3-level memory hierarchy system, the hit time for each level is
T1=10ns (L1-cache)
T2=200ns (L2-cache)
T3=600ns (Main memory)
The local hit rate in each level is H1=0.9 (L1-cache), H2=0.8 (L2-cache), and H3=1. (It is assumed that we can always find the data in main memory.) If the average access time (in ns) of this memory system is K. What is "{Round(K*123)} mod 5"?
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

6. (5 pts.) Suppose you want to perform the following executions:
(a) 100 sums of scalar variables which can only be performed sequentially
(b) A matrix sum of a pair of two-dimensional arrays, size 1000 by 1000.
What speedup do you get with 1000 processors (compared with only one processor)?
(A) 900
(B) 909
(C) 919
(D) 929
(E) 939

7. (5 pts.) Compute the clock cycle per instruction (CPI) for the following instruction mix. The mix includes 20% loads, 20% stores, 35% R-format operations, 20% branches, and 5% jumps. The number of clock cycles for each instruction class is listed as follows: 4 cycles for loads, 4 cycles for stores, 4 cycles for R-format instructions, 3 cycles for branches, 3 cycles for jumps.
(A) 3.15
(B) 3.25

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(C) 3.5
(D) 3.75
(E) 3.9

多選題（每個選項單獨計分，答錯一個選項倒扣 1 分)

8. (5 pts.) Which of the following statements are correct?
(A) The case of "TLB miss, Page Table hit, Cache hit" is possible.
(B) In a pipelined system, forwarding can eliminate all the data hazards.
(C) A write-through cache and a write-back cache will have the same miss rate.
(D) In the analysis using 3C miss model, a cache miss will be classified as one of the three types of misses, i.e. compulsory miss, conflict miss and capacity miss.
(E) Given a 32-bit long address, if a page size is 8K bytes, the virtual page number is of 19 bits long.

9. (5 pts.) For the C code A = B + C ;
Which of the following are correct.
(A) The accumulator style assembly would be
```
Load    Address(B)
Add     Address(C)
Store   Address(A)
```
(B) The memory-to-memory style assembly code would be
```
Load    R1, Address(B)
Load    R2, Address(C)
Add     R3, R1, R2
Store   Address(A), R3
```
(C) The stack-style assembly would be
```
Push Address(A)
Push Address(B)
Add
Pop Address C
```
(D) The register-to-memory style assembly code would be
```
Load    R1, Address(A)
Add     R2, R1, Address(B)
```

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Store Address(C), R2

(E) None of the above is correct.

10. (5 pts.) What of the following statements are true?
    (A) Using registers is more efficient for a compiler than other forms of internal storage.
    (B) Load interlock can be resolved by forwarding hardware.
    (C) For a cache with write through strategy, read misses might result in writes.
    (D) Compilers can schedule the instructions to avoid unnecessary hazards
    (E) None of the above

11. (5 pts.) Assume the following execution time for different operations: MUL takes 6 cycles, DIV takes 15 cycles, and ADD and SUB both take 1 cycle to complete. The instructions are issued into the pipeline in order, but out of order execution and completion is allowed. What hazards will be encountered when executing this code sequence?

```
MUL F1, F3, F2
ADD F2, F7, F8
DIV F10, F1, F5
SUB F5, F8, F2
SD   8(R1), F2
```

    (A) No hazards for this code sequence
    (B) There will be a data hazard when the ADD instruction is executed.
    (C) There will be a data hazard when the SD instruction is executed
    (D) There will be a data hazard when the DIV instruction is executed.
    (E) A Write After Read (WAR) hazard is possible when SUB instruction completes execution.

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12. (5 pts.) Which of the following instructions should be sensitive in a VM executes native instructions ?

(A) Set value of timer.
(B) Read the clock.
(C) Clear memory.
(D) Issue a trap instruction.
(E) Disable interrupts.

13. (5 pts.) Consider the following segment table:

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

What are the physical addresses reference in the following item will cause an illegal address trap to OS for the following logical addresses?

(A) 0,830
(B) 1,10
(C) 2,104
(D) 3,350
(E) 4,112

14. (5 pts.) Consider a demand-paging system with the following time-measured utilizations:

CPU utilization 20% , Paging disk 97.7%, Other I/O devices 5%

Which (if any) of the following will (probably) improve CPU utilization?

(A) Install a faster CPU.
(B) Install a bigger paging disk.
(C) Increase the degree of multiprogramming.
(D) Decrease the degree of multiprogramming.
(E) Install more main memory.

15. (5 pts.) Spinlock synchronization schemes are "not" appropriate in which system?

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(A) Single processor system
(B) Multi core system
(C) Multi-processor system
(D) Multiple computer system
(E) Real Time system

16. (5 pts.) Which of the following programming techniques and structures are good for a demand-paged environment ?
(A) Stack
(B) Hashed symble table
(C) Sequential search
(D) Binary search
(E) pure code

17. (5 pts.) A program initializes a global variable X to zero, and spawns three threads. Each of the three threads reads X, increases it by one, and then stores the result back. What are the possible values of X when all threads terminate?
(A) X = 0.
(B) X = 1.
(C) X = 2.
(D) X = 3.
(E) None of the above.

18. (5 pts.) Choose the correct statements from the multiple choices regarding context switching.
(A) Context switch time is independent of hardware support.
(B) Switching between threads of a single process is faster than switching between two separate processes.
(C) A spinlock will ultimately result in a context switch when a process must wait on a lock.
(D) Context of a process is represented in the PCB.
(E) None of the above.

19. (5 pts.) Choose the correct statements from the multiple choices regarding

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deadlock.

(A) If the resource allocation graph contains a cycle, a deadlock exists.

(B) Banker's algorithm for resource allocation deals with deadlock avoidance.

(C) There are no deadlocks if the system is in safe state.

(D) Process termination is used for deadlock prevention.

(E) None of the above.

20. (5 pts.) Choose the correct statements from the multiple choices regarding Linux.

(A) **atd** is the daemon that deals with command to be executed a single time.

(B) **cron** is the daemon responsible for executing scheduled and recurring commands.

(C) **init** is the parent of all processes.

(D) **systemd** allows more processing to be done concurrently or in parallel during system booting.

(E) None of the above.

21. (5 pts.) Choose the correct statements from the multiple choices regarding IPv6.

(A) In IPv6, routers are not allowed to fragment packets.

(B) Fragment header does not exist in IPv6 protocol.

(C) IPv6 does not support Anycast.

(D) 2001:DB8:2de::e13 is a legal IPv6 address.

(E) None of the above.