95. 3. 13

科目： 基礎電子學 應考時間：100 分鐘

1. (10 pts)

- For an OPA circuit shown in Fig. 1,

(1) Derive an expression for the transfer function $V_O(s)/V_i(s)$. Sketch the transfer function. (3 pts)

(2) If the required input resistance is 1 kΩ, design R_1, R_2 and C_2 to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz. (3 pts)

(3) At what frequency does the magnitude of transfer function become unity? What is the phase angle at this frequency? (4 pts)

2. (10 pts)

The current source circuit of Fig. 2 utilizes a pair of matched pnp transistors having $I_S = 10^{-15}$ A, $\beta = 50$, and $|V_A| = 50$ V, $V_T = 25$ mV. It is required to design the circuit to provide an output current $I_O = 1$ mA at $V_O = 2$ V.

(1) What values of I_{REF} and R are needed? Hint: $ln(10) \sim 2.3$, $ln(106) \sim 4.66$. (5 pts)

(2) What is the maximum allowed value of V_O while the current source can operate properly? (5 pts)

3. (15 pts)

A CMOS differential amplifier shown in Fig. 3 is biased with a current $I = 0.8$ mA. The design parameters are listed as follows: $(W/L) = 100$, $\mu_n C_{ox} = 0.2$ m A/V^2, $V_A = 20$ V, $I = 0.8$ mA, $C_{gs} = 50$ fF, $C_{gd} = 10$ fF, and $C_{db} = 10$ fF, $R_D = 5$ kΩ. Also, there is a 100 fF capactive load between each drain and ground.

(1) Find the overdrive voltage V_{OV} and g_m for each transistor. (5 pts)

(2) Find the differential gain A_d. (5 pts)

(3) If the input signal source has a small resistance R_{sig} and thus the frequency response is determined primarily by the output pole, estimate the 3-dB frequency f_H. (5 pts)

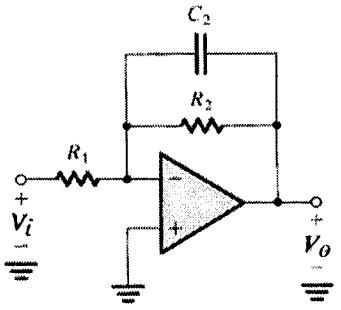

Figure 1

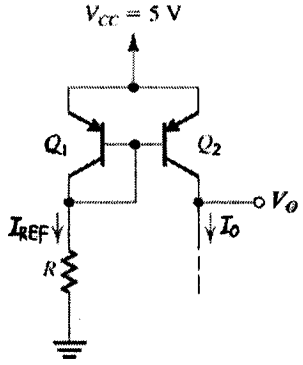

Figure 2

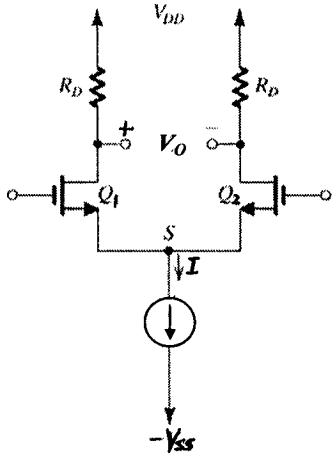

Figure 3

4. **(20 pts)**

(a) In a memory chip, how many transistors are needed for a NOR row decoder with an M-bit address? (5 pts)

(b) In a memory chip, how many transistors are needed for a tree decoder when there are 2^N bit lines? (5 pts)

(c) In a particular DRAM chip having the storage cell consists a single n-channel MOSFET and a storage capacitors C_S, if $C_S = 20$ fF, the bit-line capacitance $C_B = 0.8$ pF, the transistor V_t (including the body effect) = 1 V, $V_{DD} = 3.3$ V, estimate the output readout voltage for a stored **1** and a stored **0**. Recall that in a read operation, the bit lines are precharged to $V_{DD}/2$. (10 pts)

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5. **(15 pts)**

Find and plot the transfer characteristic for the circuit shown in Fig. 4.

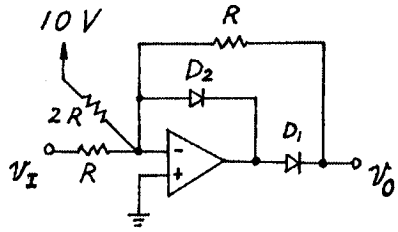
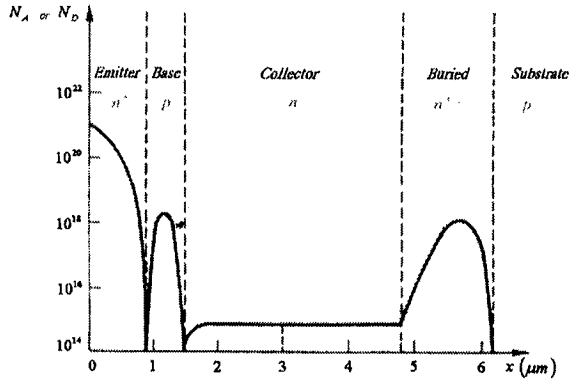


Fig. 4



垂直式npn電晶體的雜質濃度隨表面距離的關係

Fig. 5

6. **(5 pts)**

Zener diode also has the function of rectification. Is there any difference in the mechanism of rectification between forward-biased p-n diode and Zener diode? Why?

7. **(11 pts)**

Figure 5 shows a typical doping profile of an npn BJT.

(a) Can you tell me that why the emitter doping concentration is much higher than the collector doping concentration and base doping concentration? (5 pts)

(b) If you interchange the emitter and collector terminals of a BJT (i.e. the BJT is operated in reverse forward active mode), what will happen in the current gain (β), injection efficiency (α)? Why? (6 pts)

8. **(14 pts)**

(a) There are three kinds of basic structure of BJT amplifier (CE, CB, and CC). For a good current amplifier what kind of combination (which part for amplifying and which part for I/O stage) would be used? Why? (5 pts)

(b) Figure 6(a) and 6(b) show the typical i_D-v_{DS} and i_C-v_{CE} curves for a MOSFET and an npn BJT, respectively. Please answer the following questions:

1. Can you explain why the BJT has superior linearity and transconductance (g_m) to MOSFET? (5 pts)
2. What kind of MOSFET would correspond to the i_D-v_{DS} shown in Fig. 6(a)? Why? (4 pts) (Enhancement N (P) MOSFET or Depletion N (P)MOSFET)

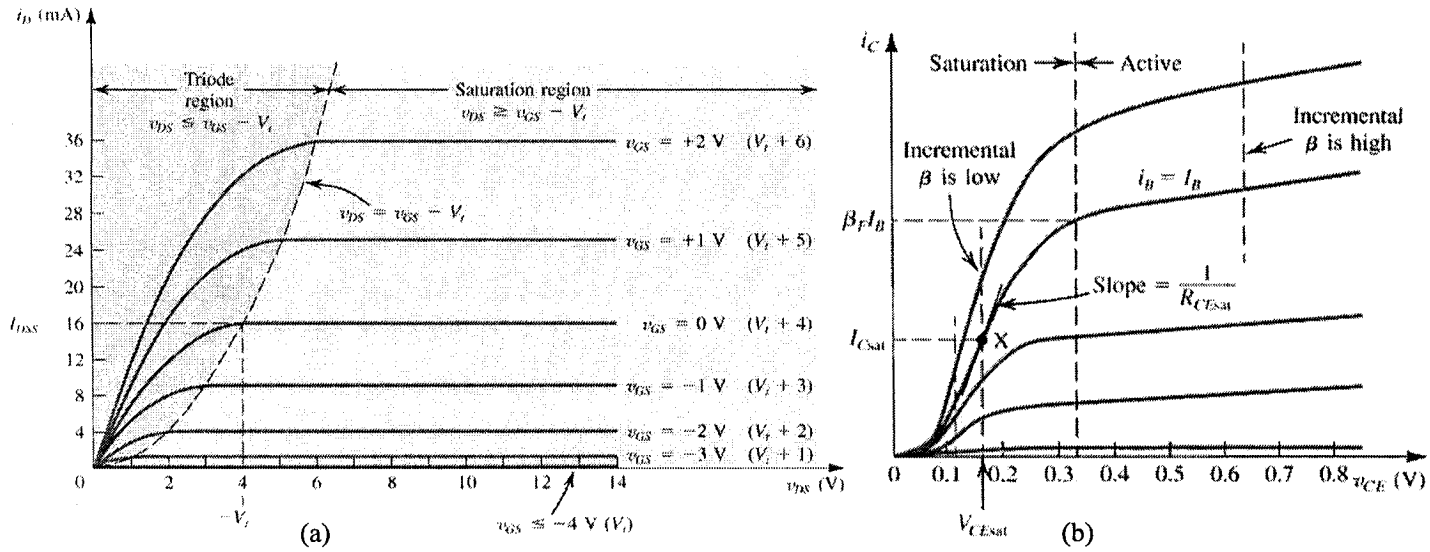


Figure 6