科目：計算機系統(計算機組織)(300B)　校系所組：中央大學通訊工程學系（乙組）
中央大學電機工程學系（電子組）
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一. [13%] Assume that the original design of a processor runs at 100 MHz clock rate and provides A, B, C instruction classes. An engineer plans to redesign the processor to be able to run at X MHz (X>100) for improvement. It is found that the CPI and usage of the instruction class for a benchmark program will be affected by the value of X in the redesigned version. The CPIs and usages of each instruction class for the original and the redesigned processor and are provided in the following table:

Instruction Class	Original Processor		Redesigned Processor	
	CPI	Usage	CPI	Usage
A	6	0.2	$6-\frac{X}{100}$	0.6
B	9	0.3	$9-\frac{X}{50}$	0.2
C	15	0.5	$15-\frac{X}{20}$	0.2

(1) [2%] What is the average CPI of the original processor?

(2) [4%] If the redesigned processor needs two times of the instruction count as the original design for the same benchmark, then what is the minimum value of X that the performance can be improved?

(3) [7%] Alternatively, we can add cache memory to improve the performance. Assume that, in average, each instruction needs 2.5 clocks for memory access in the original design and the cache access time is 5 times faster than the memory access. If we can design an ideal cache in the original processor (i.e. without any cache miss), then what is the minimum value of X for the redesigned processor (without cache) to achieve better performance than the original processor equipped with the ideal cache?

二. [12%] For each of the three MIPS instructions below:

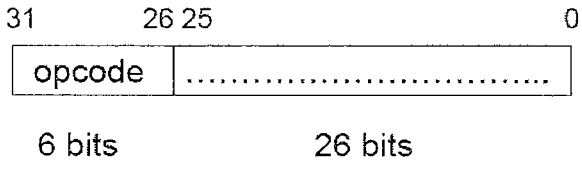
(a) `addi $15,$0,-8`

(b) `sltu $16,$15,$0`

(c) `jalr $16,$15`

[Hint] The special version of the jump-and-link instruction, `jalr rs,rd`, jumps to the address in register `rs` and puts the return address in register `rd`.

(1) [6%] Specify the machine code (**bit 0~bit 25**) of the above three instructions, respectively. You should show how many bits are in each field and leave unknown fields blank. Furthermore, you do not specify the **opcode** for above three instructions, respectively, and leave it blank.



The `rs`, `rt`, `rd` fields should be translated into binary number, respectively. For example, **$15 → 01111, $0 → 00000**. The bit codes should be written here and put in correct position.

(2) [6%] Draw the datapath and controls for a single cycle implementation of the above three instructions, respectively; only include parts of the datapath that are used in the instruction; specify the bit width of any lines you draw in the datapath, and write any known values on the lines.

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三. [13%] Suppose there exists a 12-bit IEEE 754 floating point format, with 1 sign bit, 6 exponent bits, and 5 mantissa bits.

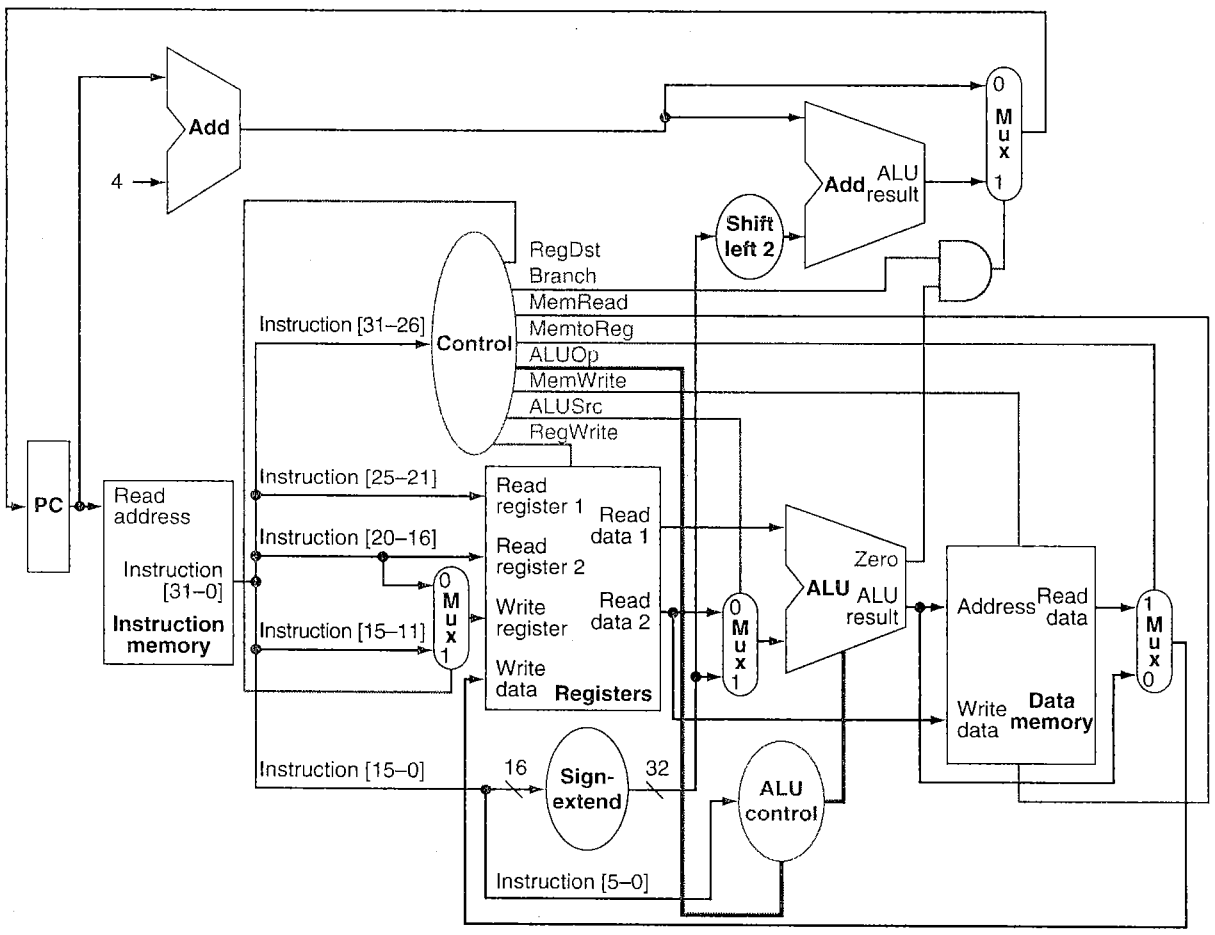
(1) [3%] How would $-\infty$ be represented in this 12-bit format? And what is the smallest positive *normalized* number? Give the value in decimal of the second number, and show both either as 12 bits or as 3 hexadecimal digits.

(2) [3%] Give the *nearest* representation n of 5.612 in this format.

(3) [2%] What is the *actual value of* n? Hence, work out its relative error r, to 3 significant digits. You may use the fact that $a/5.612 \approx a \times 0.1782$.

(4) [5%] Calculate n^2 using binary floating point multiplication. Show rounding, normalization and where you might check for overflow. Give the result as a 12-bit IEEE 754 number.

四. [25%] The simple datapath with the control unit for the MIPS processor is shown below. The input to the ALU control unit is the 6-bit opcode field from the instruction.



Consider the following instructions:

```
36: lw    $1, 50($7)
40: add   $4, $5, $6
44: sw    $4, 50($7)
48: beq   $1, $4, 8
```

(1) [5%] With the aids of the control signals, different instructions will utilize different hardware blocks of the datapath to perform the adequate function. What are the values of the 1-bit control signals

注意：背面有試題

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generated by the control unit for each instruction? Please complete the following table. Note that the input to the ALU control unit is the 6-bit opcode field from the instruction. Use "1" for true, "0" for false, and "x" for don't care.

Instruction	RegDst	ALUSrc	Memto-Reg	Reg-Write	Mem-Read	Mem-Write	Branch
add							
lw							
sw							
beq							

(2) [2%] What is the new PC address after the `beq` instruction is executed?

(3) [5%] Assume that the latencies for logic blocks in the datapath are given below:

I-Men	Add	Mux	ALU	Regs	D-Men	Sign-extend	Shift-left-2
500ps	150ps	100ps	180ps	220ps	1000ps	90ps	20ps

Assuming zero latency for the control unit, what is the clock cycle time if the processor must support `add`, `beq`, `lw`, and `sw` instructions?

(4) [3%] Suppose that the latency for ALU control block in the datapath is 55ps. To avoid lengthening the critical path, how much time can the control unit take to generate the **MemWrite** signal.

(5) [5%] For the speed-up, the processor is pipelined into 5 stages: IF, ID, EX, MEM, and WB. Please indicate what data or control dependencies affect execution of the given instructions.

(6) [5%] There are several ways to reduce the branch delay. What is the technique of the "delayed branch"? Try to re-schedule the instructions by "from-before" delayed branch scheduling, if there is a 1-cycle branch delay.

五. [5%] In the original processor shown in problem 4, some actions will be taken when an exception occurs. Please pickup the right things from the following table and give correct order about those actions. (ex: (a)->(b)->(c))

(a) stopping the execution of the program
(b) automatically execute a `jal` instruction
(c) save all register values into the stack
(d) execute the predefined actions for exceptions
(e) flushing all instructions
(f) transfer the control to OS at some specified address
(g) automatically stall one cycle
(h) save the address of the offending instruction in EPC

六. [15%] In this problem, we assume that the processor in problem 4 has been pipelined into 5 stages: IF, ID, EX, MEM, and WB with necessary pipeline registers.

(1) [6%] For the datapath shown in problem 4, please modify the datapath to implement the forwarding capability that can eliminate the stalls due the data dependency in the code sequence given in problem 4. In order to simplify the answers, only the datapath of EX and MEM stages are required to be redrawn on your answer sheet.

(2) [4%] Please explain the meanings of the added signals in (1) with the forwarding capability. The triggering conditions of the added control signals are also required.

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(3) [5%] With the forwarding capability in (1), please give the values of the control signals (**RegDst**, **ALUSrc**, **MemtoReg**, **RegWrite**, **Branch**) at the fifth cycle while executing the given code sequence in problem 4.

七. [5%] State whether the following techniques are associated primarily with a software- or hardware-based approach to exploiting ILP (Instruction-Level Parallelism). If it is associated with a software-based approach, please give an 'S' as the answer. If it is associated with a hardware-based approach, please give an 'H' as the answer. In some cases, the answer may be both.

(1) Branch prediction
(2) Register renaming
(3) Speculation
(4) Superscalar
(5) VLIW

八. [12%] Memory Hierarchy:

(1) [3%] What is the advantage of separating instruction cache and data cache when comparing to the unified cache?

(2) [3%] Please state why it is "virtual" in the so-called virtual memory?

(3) [6%] A computer system has 1G bytes main memory and 512K bytes cache with 2-way set associativity and 4-byte block size. The partial content of the cache is listed as follows at a specific time instance. Please identify the possible two lowest addresses of the data that is shaded (i.e. D2). (Note: 1…1 denotes consecutive 1s and 0…0 denotes consecutive 0s)

Index	Tag	Data(11)	Data(10)	Data(01)	Data(00)
0	100...0	81	82	83	84
	011...1	91	92	93	94
1	000...0	A1	A2	A3	A4
	011...1	B1	B2	B3	B4
2	111...1	C1	C2	C3	C4
	100...0	D1	D2	D3	D4
3	100...0	E1	E2	E3	E4
	000...0	F1	F2	F3	F4