類組：電機類　科目：數位邏輯(300H)　　　　　　　　　　※請在答案卷內作答

考生請注意：

● 本試卷共有 20 題試題。 每題 5 分。

● 你的答案必須如下圖所示由上而下依序寫在答案卷的做答區。

● 只要填寫考題所要求的答案，**請勿附加計算過程。**

從此處開始寫起
1. (a), (b).
2. (c), (d).
3. 15
4. (1) 1 ,(2) 0
5. Z = B+AC'
、、、

注意:背面有試題

※請在答案卷內作答

Question 1 [5pt]. Convert $(25.375)_{10}$ to binary.

Question 2 [5pt]. Determine the base of the number system in each case for the following operations to be correct:

(a) $39 + 59 = 91$

(b) $18 * 25 = 378$

Question 3 [5pt]. For the Boolean function $F = (u' + y)(u' + y')(u + x + y'z)$, use Boolean algebra to simplify the function to a minimum sum of products.

Question 4 [5pt]. Simplify the following Boolean expression to three literals: $A'C' + ABC + AC'$, and find the **complement** of the simplified result.

Question 5 [5pt]. Which of the following equations are NOT VALID.

(a) $(a+b)(b+c)(c+a) = (a'+b')(b'+c')(c'+a')$

(b) $abc + ab'c' + b'cd + bc'd + ad = abc + ab'c' + b'cd + bc'd$

(c) $xy' + x'z + yz' = x'y + xz' + y'z$

(d) $x'y + y'z + z'x = xy' + yz' + zx'$

Question 6 [5pt]. $f(A, B, C, D) = AC + ABC' + BC'D$. What is the minimum number of 2-to-1 multiplexor to implement function f?

Question 7 [5pt]. How many NOR gates are needed to implement a minimum two-level, multiple-output NOR-NOR circuit that realizes the following two functions?
$f_1 = \Sigma m(0, 2, 4, 6, 7, 10, 14)$ and $f_2 = \Sigma m(0, 1, 4, 5, 7, 10, 14)$

Question 8 [5pt]. Which of the following transitions are possible hazards for the circuit? Please specify all of them.
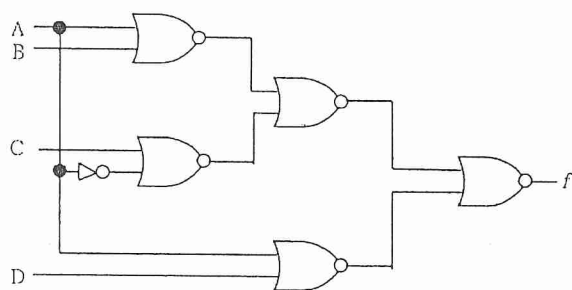
(A) $0001 \leftrightarrow 1001$　(B) $0011 \leftrightarrow 1011$　(C) $0000 \leftrightarrow 1000$　(D) $0010 \leftrightarrow 1010$

Question 9 [5pt]. Continue on Question 8, please redesign the circuit with a minimum two-level NOR-NOR circuit that is free of all hazards. How many inputs are needed for the NOR gate that generates output f?
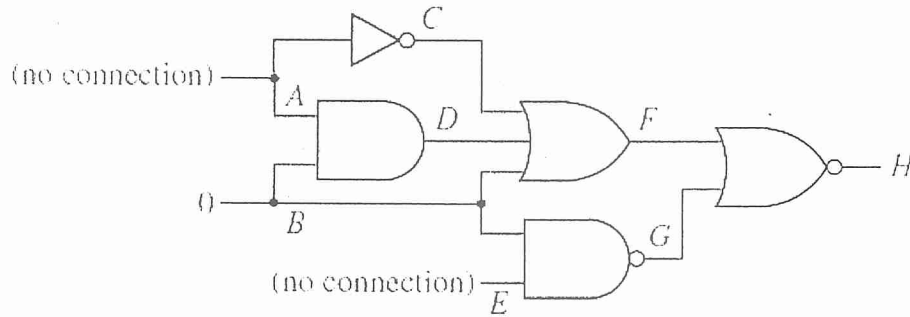
注意：背面有試題

Question 10 [5pt]. The function $F = CD'E + CDE + A'D'E + A'B'DE' + BCD$ is implemented in an FPGA with $F = A'C'(F_0) + A'C(F_1) + AC(F_3)$. Please write down the minterm expressions of the three-variable functions $F_0(B,C,D)$, $F_1(B,C,D)$, and $F_2(B,C,D)$.

Question 11 [5pt]. Using four-valued logic, find (A, D, F, H).

Question 12 [5pt]. A two-level, NOR-NOR circuit implements the function.

$$f(a, b, c, d) = (a + d')(b' + c + d)(a' + c' + d')(b' + c' + d).$$

Find all static-0 hazards for $(a, b, c, d) = (0, 1, 0, 0)$ in the circuit.

Question 13 [5pt]. Expand the following function about the variable b.

$F = ab'cde' + bc'd'e + a'cd'e + ac'de'$

$= b'(\underline{\hspace{2cm}}) + b(c'd'e + a'd'e + ac'de')$

Question 14 [5pt]. A full adder is implemented using two 4-to-1 MUXes. Connect X and Y to the control inputs of the MUXes, and connect 1, 0, C_{in}, or C_{in}' to each data input. Please write the correct inputs for ports (a, b, c, d).
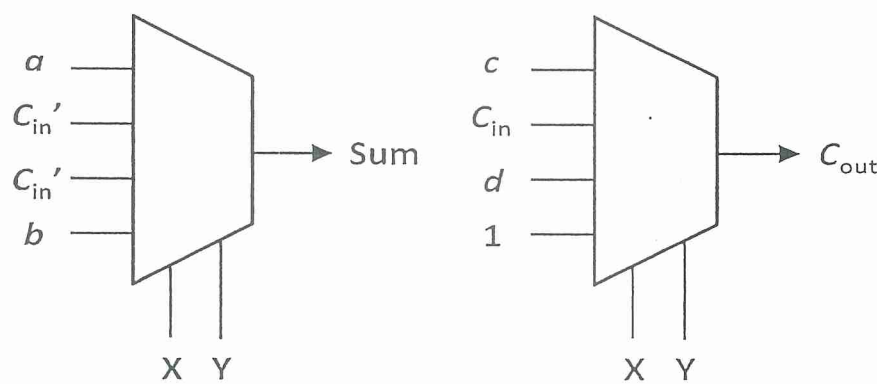
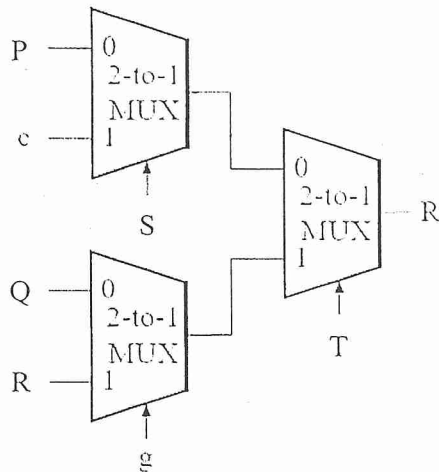**Question 15 [5pt].** Implement the following function using only 2-to-1 MUXes:

$$R = ab'h' + bch' + eg'h + \_fgh.$$

Please write the correct inputs for ports (P, Q, R, S, T).

Question 16 [5pt]. Below is an incompletely specified state table with 6 states.

Present	Next State		Output	
State	X= 0	1	X= 0	1
S0	S2	S4	1	0
S1	S0	S1	1	1
S2	S3	S5	1	1
S3	-(1)	S1	0	0
S4	S2	-(2)	0	0
S5	S2	S3	-(3)	0

How to specify the three don't-care bits denoted as (1), (2) and (3), respectively, in the state table such that the number of states in the state table can be reduced to four?

Question 17 [5pt]. Following shows the stage graph of a circuit with two inputs (denoted as X and Y) and one output (denoted as Z). Then we implement the state graph with three D flip-flops (denoted as Q_2, Q_1, and Q_0) and the one-hot state assignment, where $S_0(Q_2Q_1Q_0):001$, $S_1(Q_2Q_1Q_0):010$, and $S_2(Q_2Q_1Q_0):100$. What are the equations for Q_2^+, Q_1^+, and Q_0^+, respectively, under this situation?
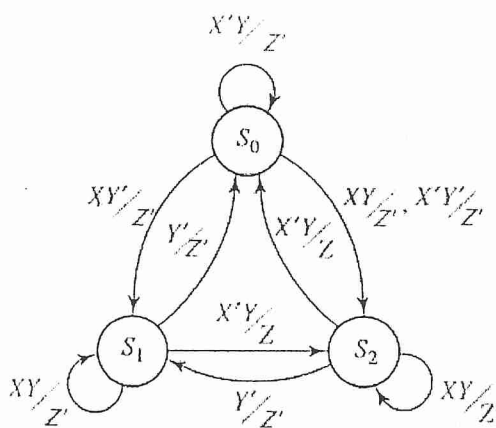
注意：背面有試題

Question 18 [5pt]. Please identify which of the following five circuits, from Circuit(B) to Circuit(F), are equivalent to circuit (A).

Circuit(A)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{A0}	S_{A0}	S_{A2}	1
S_{A1}	S_{A3}	S_{A0}	0
S_{A2}	S_{A2}	S_{A1}	1
S_{A3}	S_{A1}	S_{A3}	0

Circuit(D)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{D0}	S_{D0}	S_{D1}	1
S_{D1}	S_{D3}	S_{D2}	0
S_{D2}	S_{D2}	S_{D4}	1
S_{D3}	S_{D1}	S_{D3}	0
S_{D4}	S_{D0}	S_{D1}	1

Circuit(B)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{B0}	S_{B2}	S_{B3}	1
S_{B1}	S_{B1}	S_{B0}	0
S_{B2}	S_{B2}	S_{B0}	1
S_{B3}	S_{B1}	S_{B3}	0

Circuit(E)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{E0}	S_{E3}	S_{E4}	1
S_{E1}	S_{E0}	S_{E3}	0
S_{E2}	S_{E4}	S_{E2}	1
S_{E3}	S_{E1}	S_{E0}	0
S_{E4}	S_{E2}	S_{E1}	1

Circuit(C)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{C0}	S_{C3}	S_{C0}	0
S_{C1}	S_{C1}	S_{C2}	1
S_{C2}	S_{C2}	S_{C3}	1
S_{C3}	S_{C0}	S_{C1}	0

Circuit(F)

Present states	Next states		Output (Z)
	X=0	X=1	
S_{F0}	S_{F4}	S_{F3}	1
S_{F1}	S_{F5}	S_{F1}	0
S_{F2}	S_{F2}	S_{F4}	1
S_{F3}	S_{F1}	S_{F2}	0
S_{F4}	S_{F4}	S_{F5}	1
S_{F5}	S_{F1}	S_{F2}	0

注意：背面有試題

Question 19 [5pt]. Below is a state transition table with 8 states.

ABC	Next State $A^+B^+C^+$ X = 0	1	output Z X = 0	1
000	111	011	1	1
010	101	001	0	0
100	001	101	1	0
110	011	111	0	0
111	001	001	0	0
001	100	000	1	0
101	011	111	0	1
011	110	110	1	0

If we implement the state table using 3 T flip-flops as shown in the following figure, what is the input equation of T_A?
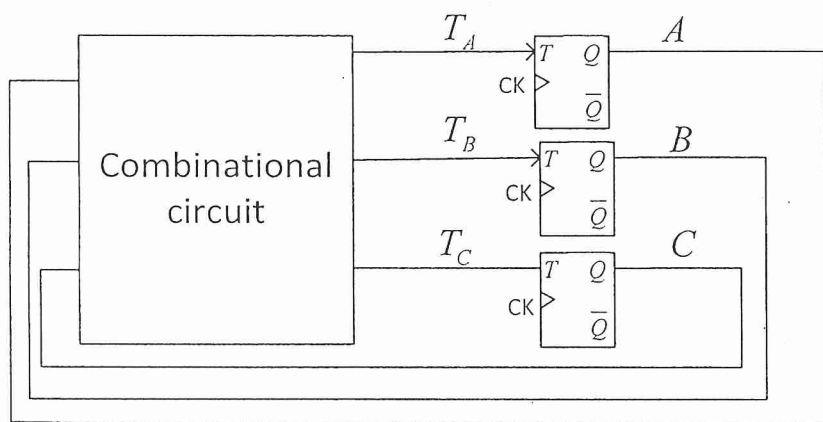
Question 20 [5pt]. The targeted Mealy machine has one input (X) and one output (Z). The value of output Z is equivalent to the value of input X two clock cycles before. The values of output Z at the first two clock cycles are all zero. Following table shows an exemplary input/output sequence of the targeted mealy machine.

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	0	1	1	0	0	0	1	0	1	0	0	1	1	1	0	1
Z	0	0	0	1	1	0	0	0	1	0	1	0	0	1	1	1

Following is the corresponding state table of the targeted Mealy machine with some missing slots. Please list the missing slots (a), (c), and (e), respectively.

Present states	Next states		Output (Z)	
	X=0	X=1	X=0	X=1
S_0(Reset)	S_1	S_2	0	0
S_1	S_1	(a)	0	0
S_2	(b)	(c)	0	0
S_3	S_1	S_2	(d)	(e)
S_4	S_3	S_4	1	1