科目：電子學(5001)　　參考用

校系所組：中大光電科學與工程學系、照明與顯示科技研究所
清大電機工程學系甲組、乙組、丙組、丁組
清大光電工程研究所、電子工程研究所、
清大工程與系統科學系丁組、動力機械工程學系乙組
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1. Consider the common-emitter amplifier circuit of Fig. 1 with a supply voltage V_{CC} = 10V. Assume that the BJT has $I_S = 10^{-15}$A, $\beta = 100$, $C_\mu = 0.2$ pF, and C_π = 1pF.

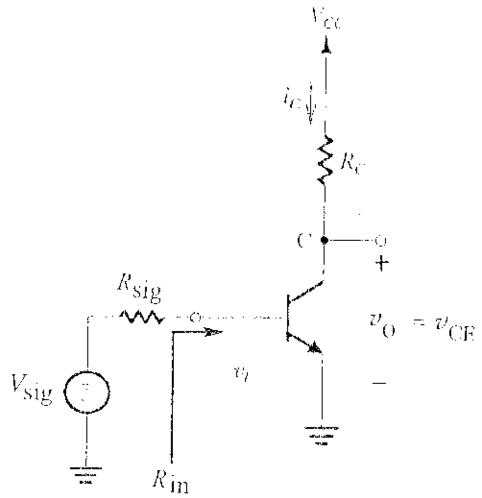

Fig. 1

(a) Biasing the BJT with a dc collector current I_C = 1mA, find dc voltage V_{BE} and R_C to provide a voltage gain v_O / v_{be} = -100V/V (5%).

(b) Find the incremental (or small-signal) input resistance R_{in} and the input capacitance C_{in} of the amplifier. (5%)

(c) With R_{sig} = 1KΩ, find the -3dB bandwidth f_H and unity-gain bandwidth f_T of v_O / v_{sig}. (5%)

2. The parameters of the circuit shown in Fig. 2 is listed below:

V_{th} = 1 V, $\mu_n C_{ox}$ = 100 μA, λ = 0, and L1 = L2 = L3 = L4 = 1um
W1 = 8um, W2 = W3 = W4 = 32um

(a) Find the voltage values at nodes V1, V2, and V3. (Neglect the body effect and channel length modulation) (15%)

(b) What operation regions are Q1 and Q3 in (cutoff, saturation or triode)? (5 %)

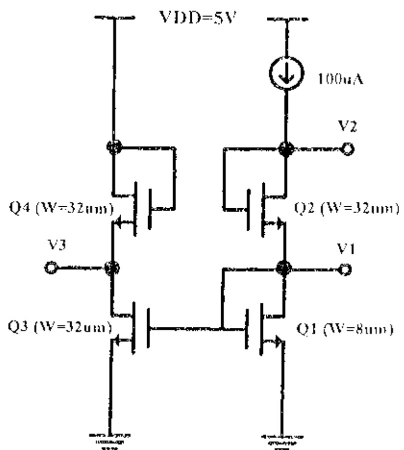

Fig. 2

注意：背面有試題

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3. Find the input impedance $Z_{in} = V/I$ of the op-amp circuit shown in Fig. 3. (15%)

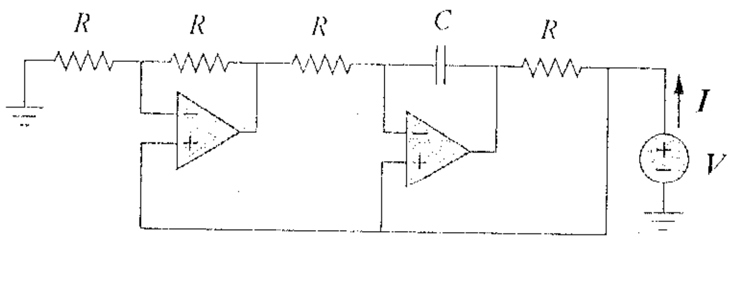

Fig. 3

4. For the op-amp circuit shown in Fig. 4, if $v_1(0^+) = 5$ V and $v_2(0^+) = 0$ V, find v_o for $t > 0$. Let $R_1 = 100$ KΩ, $R_2 = 200$ KΩ, $C_1 = 1\mu F$, $C_2 = 0.5\ \mu F$. (15%)

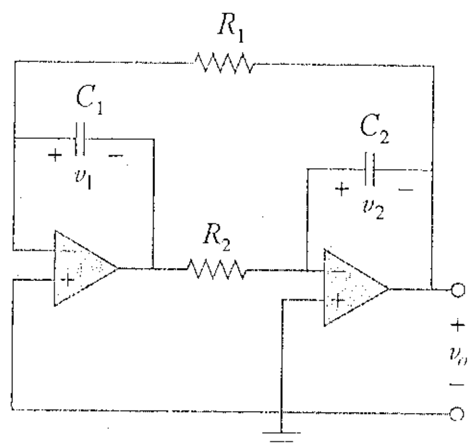

Fig. 4

注意：背面有試題

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5. Fig. 5 shows a popular configuration for a two-stage CMOS OP Amp. Assuming the transconductances of $Q_1 \ldots Q_8$ are $g_{m1} \ldots g_{m8}$, the output resistances of $Q_1 \ldots Q_8$ are $r_{o1} \ldots r_{o8}$, answer the following questions to analyze its operation and design its compensation network.

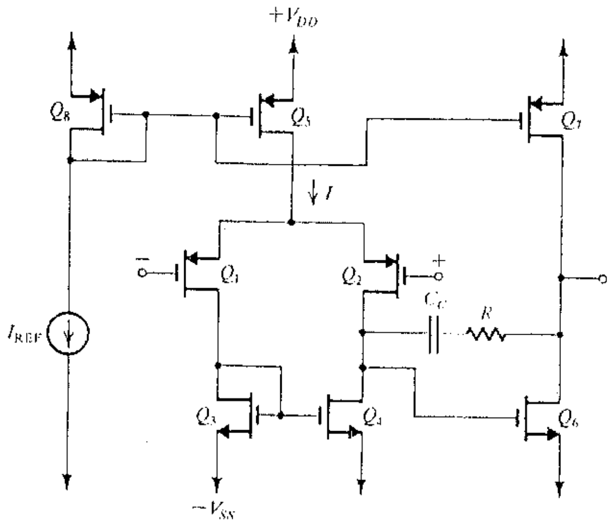

Fig. 5

(a) Find out the overall DC voltage gain of the CMOS OP Amp. (5%).

(b) Assume that the load capacitance C_L **and** C_C **are much greater than the transistor capacitances**. Then we can find the CMOS OP Amp to have two poles ω_{P1}, ω_{P2} and one zero ω_Z such as:

$$\omega_{P1} \cong \frac{1}{G_{m2} R_1 R_2 C_C} \qquad \omega_{P2} \cong \frac{G_{m2}}{C_L} \qquad \omega_Z = \frac{G_{m2}}{C_C}$$

where G_{m2} is the transconductance of the second stage, R_1 is the output resistance of the first stage, R_2 is the output resistance of the second stage. If we already know the unity gain frequency f_t, what is the phase margin of the Op Amp in terms of f_t, f_{P2}, f_Z .(5%)

(c) The additional phase lag provided by the zero is unwanted. A simple and elegant solution is to include a resistance R in series with C_C, as shown in Fig. 5. If we want to place the zero at infinite frequency, how should we pick the value of resistance R_∞? (5%)

(d) Suppose student A selects $R = R_A > R_\infty$ and gets phase margin PM_A, student B selects $R = R_B < R_\infty$ and gets phase margin PM_B, student C selects $R = R_\infty$ and gets phase margin PM_C. Please compare their phase margins. (5%)

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6. The circuit shown in Fig. 6 (a) can be used as a memory element. The output voltage with only two possible states L^+ and L^- is determined by the previous value of the trigger signal V_{in}, where R_1= 2 kΩ and R_2= 10 kΩ:

(a) Assuming L^+= 12 V and L^-= -12 V, determine the input threshold voltages V_{TH} and V_{TL} when the output state changes. (5%)

(b) By adding R_3 (2 kΩ) and V_{ref} (12 V), the circuit shown in Fig. 6 (b) becomes a comparator with hysteresis characteristics. Determine the threshold voltage V_{TH} and V_{TL}, and plot the transfer characteristic V_{in}/V_{out} of the circuit. (10%)

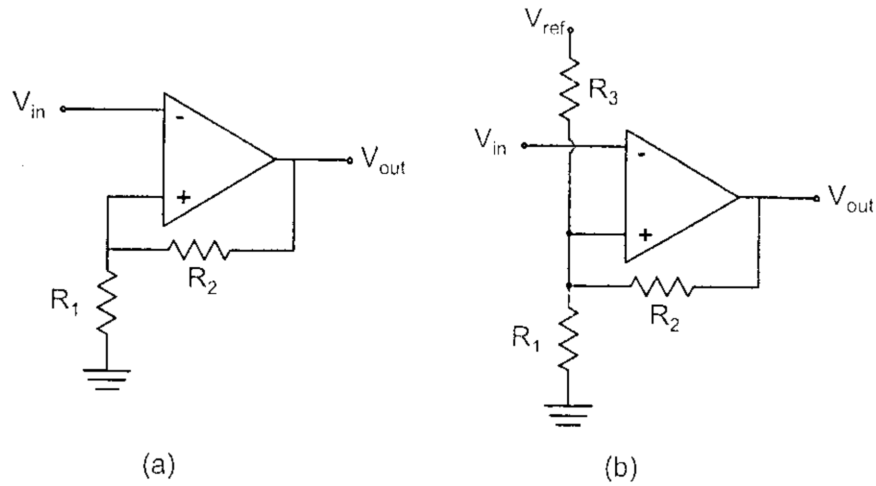

Fig. 6