## 國立中央大學95學年度碩士班考試入學試題卷 #\_4\_頁 第\_/\_頁

# 所別:<u>資訊工程學系碩士班</u>科目:<u>作業系統與計算機組織</u> <u>軟體工程研究所碩士班</u>

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1. (15%) Consider the following page-reference string: 1,2,3,4,2,3,1,5,6,5,2,1,2,3,5,7,6,3,4,5,2,1,2,3,6,7

How many page faults would occur for the following replacement algorithms, assuming three, six, or seven frames? Remember that all frames are initially empty, so your first unique pages will all cost one fault each.

- (a) LRU replacement
- (b) FIFO replacement
- (c) Optimal replacement
- 2. (20%) Consider the following program fork.c in UNIX (FreeBSD) operating system:

```
1 #include <stdio.h>
 2 main(int argc, char *argv[])
 3 {
 4 int pid;
      pid = fork();
      if (pid < 0) {
 6
 7
          fprintf(stderr, "Fork Failed");
 8
          exit(-1);
 9
10
      else if (pid == 0) {
      printf("Before /bin/ps \n");
11
12
      execlp("/bin/ps", "ps", "-x");
13
14
         else {
15
          printf("Before Wait \n");
16
          wait(NULL);
17
          printf("Child Complete \n");
18
          exit(0);
19
20 }
```

After compiling & execution, the result is showing as: bash-2.03\$ cc fork.c -o ex-fork bash-2.03\$ ./ex-fork
Before Wait

注:背面有試題

## 國立中央大學95學年度碩士班考試入學試題卷 #\_4\_頁 第 2 頁

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```
Before /bin/ps
PID TT STAT TIME COMMAND
61469 p1 Ss 0:00.21 -bash (bash)
61500 p1 S+ 0:00.01 ./ex-fork
61501 p1 R+ 0:00.00 ps -x
Child Complete
```

bash-2.03\$

Please answer the following questions:

- 1. After line 5 fork() statement, what will happen when this program is executed?
- 2. Does process with PID 61500, 61501 share the same execution environments? Before line 12 execlp() statement is executed, which two processes shared the same memory space?
- 3. Describe the advantages of technique "Copy on write"
- 4. Considering the stack and heap operation, describe the advantages of technique "zero-fill-on-demand".
- 3. (15%) The critical-section problem is solved by defining two atomic operation wait( or P operator from the Dutch proberen, to test) and signal ( or V operation; from verhogen, to increment) with counting semaphore S (an integer variable)

- 1. Why the wait and signal operations should be executed atomically? Please show it is necessary.
- 2. The mutual-exclusion solution with semaphore definition requires busy waiting for wait(s) (P-operation), to overcome the waste CPU cycles of busy waiting in single processor system, a technique called "block itself" is used, Please write the semaphore as a C struct and using block() and wakeup(Process) basic kerne-system-call operation to implement it.
- 3 Describe the major function and advantages using the technique of "spinlock" in multiprocessor system.
- 4. Explain these terms in Solaris 2: adaptive mutex, turnstile, priority inversion and priority inheritance protocol

# 國立中央大學95學年度碩士班考試入學試題卷 #\_4\_頁 第\_3\_頁

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P3

4.(10%)There are two machines, M1 and M2, run the same instruction set. The instruction set is composed of 3 classes of instructions (A, B, and C). M1 runs at 100 MHz, and M2 runs at 250 MHz. The average number of cycles per instruction for each implementation are as follows:

Instruction Class	CPI of M1	CPI of M2
A	1	2
В	1	2
С	3	2

(1)(5%) Define the peak performance as the fastest rate at which a machine could execute an instruction sequence chosen to maximize the rate. What are the peak performances of M1 and M2 in instructions per second?

(2)(5%) If a benchmark program consists of 30%, 30%, and 40% of all instructions for class A, B, and C, respectively. Which machine will execute the program faster, and by how much?

5.(15%)Consider a 6-stage pipeline, if it needs two clock cycles in stage 3 and three clock cycles in stage 4, while each of the other stages only needs one clock cycle.

- (1) (5%) Please draw a figure to indicate the execution flow of 5 instructions for the above pipeline machine in ideal case (without any hazard).
- (2) (5%) Please specify the number of clock cycles that is required to execute *n* instructions for the above pipeline machine in ideal case (without any hazard).
- (3) (5%) Please use figure to explain how the superscalar technique can be applied to improve the performance of the above pipeline machine?

#### 6. [25%]

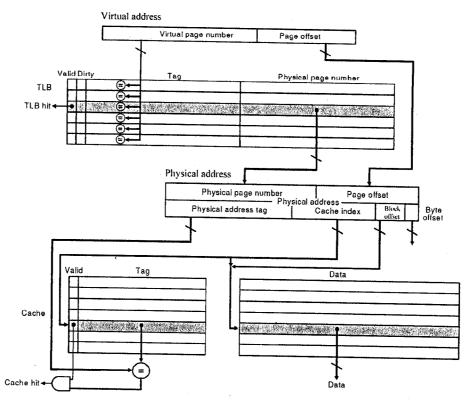
You are designing a memory system similar to the one shown in the following figure: Your memory system design uses 16KB pages, 40-bit virtual byte address and 32-bit physical address. The TLB contains 16 entries. The cache has 4K blocks with 4-word block size (1 word has 4 bytes) and is 4-way set associative.

注:背面有試題

### 國立中央大學95學年度碩士班考試入學試題卷 共 4 頁 第 4 頁

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P4.



- (a) What is the total size of the physical page number in the page table for each process on this processor? (Assuming that all the virtual pages are in use.)
- (b) What is the total number of tag bits for the cache?
- (c) What kind of associativity (direct-mapped, full-associative or set-associative) will you choose for this TLB and why?
- (d) Assume that you choose 2-way set associativity for TLB and that each block has 4 words and the initial TLB is empty. After a series of address references given as word addresses: 1, 4, 8, 5, 17, 32, 19, 1, 56, 9, 25. Please label each reference in the list as hit or miss. (Note: The first word address of each block is a multiple of 4 and LRU is used.)
- (e) A memory reference in this system may encounter three types of misses: a TLB miss, a page fault and a cache miss. Consider all the 8 combinations of the three events (with hit/miss) and identify/explain which cases are impossible.
- (f) To improve the cache performance, you are allowed to change (i) cache size (ii) associativity (iii) block size. Please describe their positive and negative affects on the performance.