國立中央大學九十一學年度碩士班研究生入學試題卷

所別：資訊工程學系 不分組 科目：計算機結構 共 1 頁 第 1 頁
網路學習科技研究所 甲組

1. 詳細解釋下列名詞或回答下列問題 (每小題 5 分，合計 45 分)

   (a) What are the 2 types of control unit design?

   (b) What are the 3 types of control signals that a control unit should generate?

   (c) Given an 8-bit 2's complement representation ($x_7\ x_6\ \ldots\ x_1\ x_0$). What's the value that it represents by writing down the equation?

   (d) Two-bit dynamic branch prediction.

   (e) Describe the basic idea of Booth's multiplier and especially the conversion table.

   (f) What's the "latency" of a pipeline?

   (g) What's the "throughput" of a pipeline?

   (h) Superscalar processor

   (i) Cache coherence

2. Explain the 3 types of possible data dependency problems. (10 分)

3. A non-pipelined processor X has a clock rate of 100 MHz and an average CPI of 4. Processor Y, an improved successor of X, is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 75 MHz. If a program containing 1000 instructions is executed on both processors, what is the maximum speedup of processor Y compared with that of processor X? (10 分)

4. Develop a 4-bit cyclic shift right register using 4 S-R flip-flops. (10 分)

5. Design a 4-bit*4-bit 2's complement multiplier using a ROM in a most economical way, i.e., to use as few input lines and out lines as possible. (10 分)

6. In the IEEE 754 floating-point number representation standard:

   (a) Describe the format of the standard, including its representation range, underflow and overflow conditions. (10 分)

   (b) Write down the IEEE 754 representation (in hex format) for "–13.125" (5 分)