所別：電機工程學系碩士班 甲組(一般生) 科目：計算機組織
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1. (a). (9 points) Assume variable h is associated with register $s2 and the base address of the array A is in $s3. Now the C assignment statement is as below:

   `A[12] = h + A[8]`

   Write the compiled MIPS assembly code by filling the blanks (A), (B), (C).

   ```
   lw   $t0, __(A)__($s3)
   add  ___(B)__, ___(C)__, $t0
   sw   $t0, 48($s3)
   ```

   (b). (3 points) If the program is run with a machine of 50 MHz clock, and it needs to execute the code in (a) for 10000 times. Below is the number of cycles for each class of instruction. How many ms (micro seconds) will it take to execute this program?

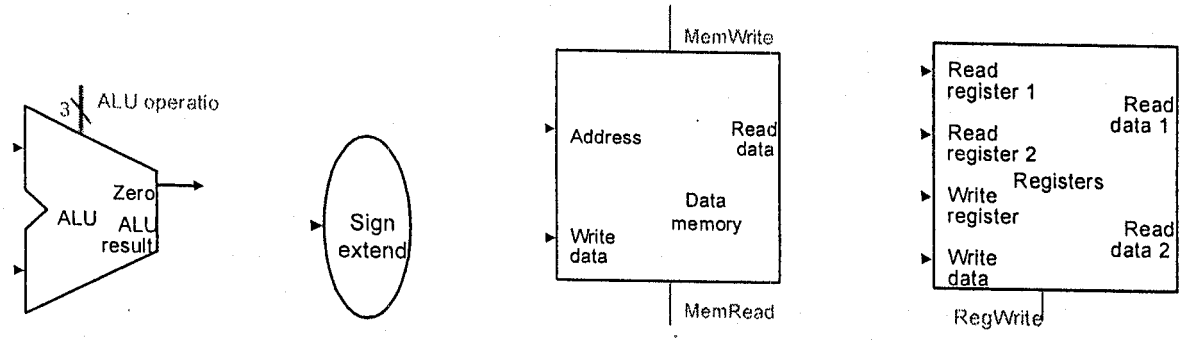
Instruction	Cycles
Arithmetic	1
Data transfer	3
Jump	2

   (c). (3 points) If the machine in (b) is a 4-way VLIW machine, what is the MOPS (million operations per second) of this machine?

2. (a). (5 points) A PC has 4 MB of RAM beginning at address 00000000H. Calculate the very last address (in hex) of this 4 MB block.

   (b) (5 points) If the starting address and the ending address of the ROM block are 008000H and 010000H, calculate the size of the ROM in K.

3. (5 points) Please draw the block diagram to build a simple MIPS datapath, only using the following four components: "ALU", "Sign extend", "Data memory", "Registers".



4. (a). (5 points) Use the block diagram of 1-bit full adder as a basic block to construct a 32-bit ripple adder (S=A+B).

   (b). (5 points) Add some logic blocks to the design of ripple adder so that it can do 2's complement subtraction (S=A-B).

   (c). (5 points) Using 4-bit carry-lookahead blocks to form a 16-bit carry- lookahead adder. Draw the block diagram and write down the corresponding logic equations.

   (d). (5 points) Compare the number of "gate delays" for the critical paths of two 16-bit adders, one use ripple carry and one using two-level carry lookhead.

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5. (a). (20 points) Figure 5.1 shows the partial finite state machine with control line settings to control the datapath in Figure 5.2. Figure 5.2 below shows the MIPS multicycle datapath with exception handling. Please fill in the names and values of the control lines that need to be changed in the empty states A to E such that the finite state machine can control the datapath correctly.

(b). (6 points) Assume only one exception, arithmetic overflow, can occur in this MIPS CPU. Please redraw the finite state machine to handle this exception using the datapath shown in Figure 5.2.

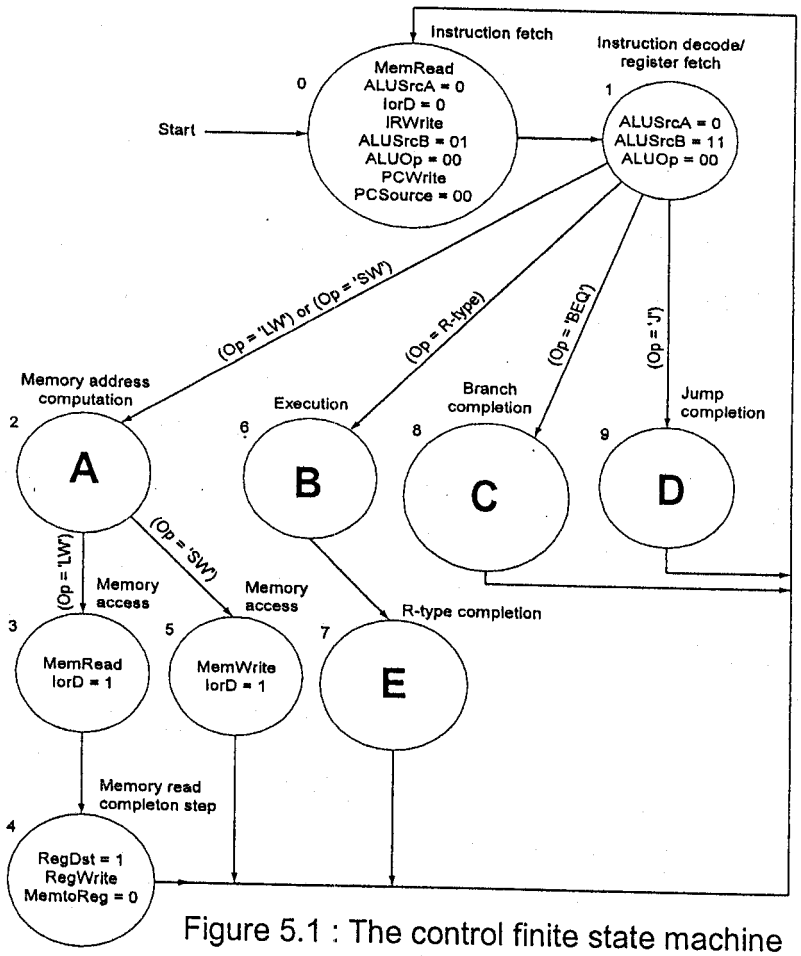

Figure 5.1 : The control finite state machine

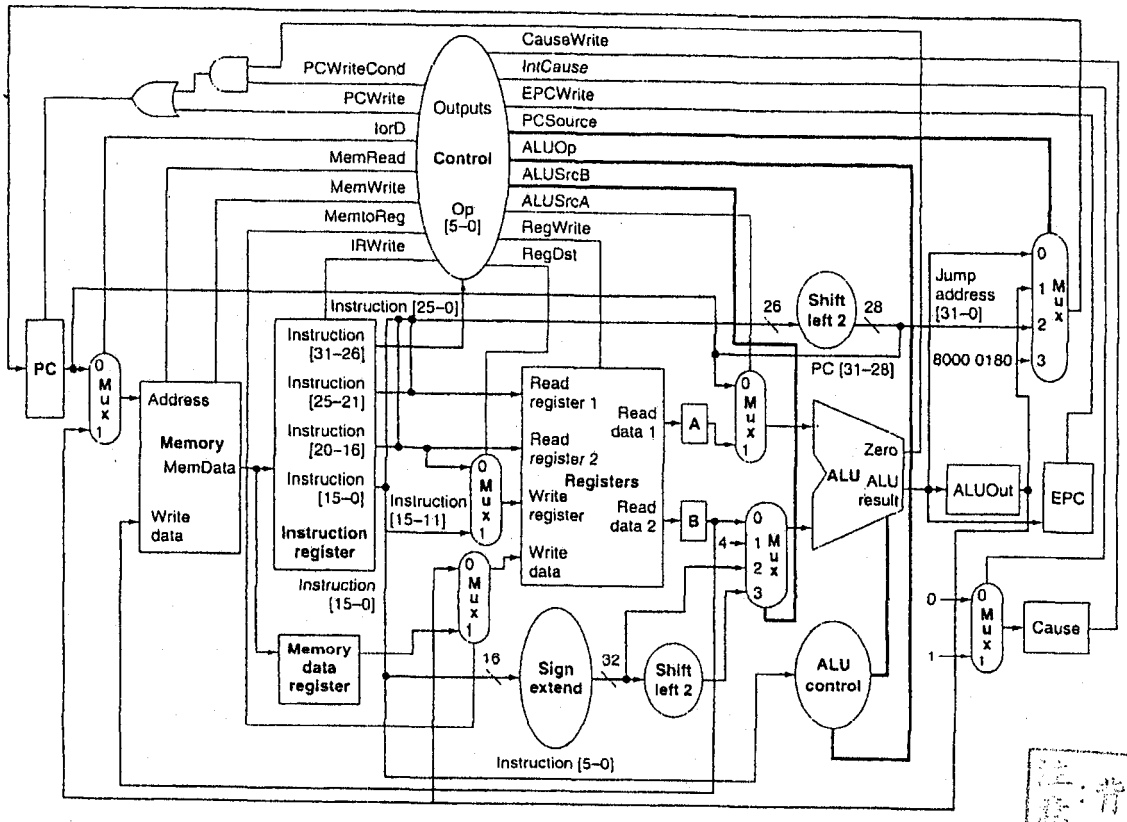

Figure 5.2: The multicycle datapath for problem 5.

注意：背面有試題

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6. (a). (4 points) While executing the MIPS code shown right, what is the target address of the branch instruction if it is taken? (Assume the starting address of this code segment is $28_{dec.}$)

```
lw   $4, 50($7)
beq  $1, $4, 3
add  $5, $3, $4
sub  $6, $4, $3
or   $7, $5, $2
slt  $8, $5, $6
.....
```

(b). (8 points) Assume this code is executed on a MIPS CPU with 5 pipeline stages and data forwarding capability. If this CPU uses "always assume branch not taken" strategy to handle branch instruction but the branch is taken in this example, how many clock cycles are required to complete this program? Please explain your answers in detail.

7. (a). (6 points) Please briefly explain the relationship between virtual memory, TLBs, and caches in the memory system of modern computers.

(b). (6 points) Assume there are two small caches, each consisting of six one-word blocks. One cache is direct mapped, and the other cache is two-way set associative. Please find the number of misses of each cache organization given the following sequence of block address: 0, 15, 12, 3, 15, 0. Besides the number of misses, please also explain your answers in detail.