

類組：電機類 科目：計算機系統(計算機組織)(300A)

※請在答案卷內作答

一. [12%] Consider a virtual memory system with the following characteristics:

- Page size of 64 KB = 2^{16} bytes
- Page table and page directory entries of 8 bytes per entry
- Inverted page table entries of 16 bytes per entry
- 31 bit physical address, byte addressed
- Two-level page table structure (containing a page directory and one layer of page tables)

- (1) [6%] What is the size (in number of address bits) of the virtual address space supported by the above virtual memory configuration?
- (2) [6%] What is the maximum required size (in KB, MB, or GB) of an inverted page table for the above virtual memory configuration?

二. [13%] Consider two different implementations, M1 and M2, of the same instruction set. There are four classes of instructions (A, B, C and D) in the instruction set. M1 has a clock rate of 100 MHz and M2 has a clock rate of 150 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

| Instruction Class | Machine M1 – Cycles/Instruction Class | Machine M2 – Cycles/Instruction Class | Frequency |
|-------------------|---|---|-----------|
| A | 1 | 2 | 40% |
| B | 2 | 3 | 10% |
| C | 4 | 4 | 30% |
| D | 6 | 6 | 20% |

- (1) [4%] Calculate the average CPI for each machine, M1, and M2.
- (2) [4%] Calculate the average MIPS ratings for each machine, M1 and M2.
- (3) [5%] Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS?

三. [10%] Assume we are designing a 16-bit MIPS CPU with 16-bit instruction words.

- (1) [3%] Assume the IEEE-754 floating-point representation is also adjusted to 16-bit long for this 16-bit MIPS CPU. If the exponent is 6-bit and the mantissa is 9-bit in this 16-bit floating-point format, what is the maximum number that it can represent? Please use base-10 scientific notation to show your answer. (assume $\log_{10}2 = 0.3$)
- (2) [2%] In the IEEE-754 floating-point representation, the exponent field employs the *excess-N* coding. What should be *N* in your 16-bit floating-point format if it follows the similar mechanism?
- (3) [5%] Given two decimal numbers 6.25 and -3.375. Please translate them into the 16-bit floating-point format specified in (1) and calculate the sum of the two numbers using floating-point addition. Assume that we can store only four digits of the mantissa fields during the addition. Because no extra guard and round bits are available, the digits exceeding 4 bits will be truncated.

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四. [15%] Assume variable sum is passed with register \$a0. Therefore, the following C program segment can be converted to the MIPS assembly code as shown right.

```
int sum (int n) {
    if (n < 1) return 0;
    else return (n + sum(n-1));
}
```

```
Sum: addi $sp,$sp,(a)
      sw  $ra,4($sp)
      sw  $a0,0($sp)
      slti $t0,$a0,1
      beq $t0,$zero,L1
      add $v0,$zero,(b)
      addi $sp,$sp,8
      jr  $ra
L1:   addi $a0,$a0,-1
      jal Sum
      lw  $a0,0($sp)
      lw  $ra,4($sp)
      addi $sp,$sp,8
      (c) $v0,$a0,$v0
      jr  $ra
```

- (1) [6%] Please fill in the blanks (a), (b), (c) to complete this assembly code.
- (2) [2%] Assume the initial values of \$a0, \$t0, \$v0 are 5, 6, 7, respectively. What is the final value of \$v0 after this code is finished?
- (3) [3%] Please translate the instruction `lw $ra,4($sp)` to machine code in hexadecimal form. (`lw` → opcode=35, `$sp` → 29, `$ra` → 31)
- (4) [4%] Assume the current PC value is 0x20406080 while starting the execution of this code, what values should be filled into the address fields of the instructions `beq $t0,$zero,L1` and `jal Sum` respectively?

五. [15%] Please describe the following terms concerning computer architecture

- (1) [5%] What are the instruction-level parallelism (ILP), out-of-order (OOO) execution, and multi-issue processor? How to guarantee precise interrupt in a multi-issue superscalar processor?
- (2) [5%] Please describe at least four different ways to update the PC in the simplified MIPS. Both an exception and a jal instruction can change the program flow and then return. What is the major difference between them?
- (3) [5%] Why should the operands of arithmetic instructions come from registers instead of memory in modern processors? Why should the number of available registers be limited? Briefly describe at least 3 reasons.

六. [10%] With pipelining, many instructions are simultaneous executing in a single datapath in every clock cycle. Consider the following instruction sequence:

```
lw    $t1, 0($t0)
lw    $t2, 4($t0)
add   $t3, $t1, $t2
sw    $t3, 12($t0)
lw    $t4, 8($t0)
add   $t5, $t1, $t4
sw    $t5, 16($t0)
```

For the classical MIPS with 5-stage pipeline datapath,

- (1) [2%] Find the hazards in the given code segment.
- (2) [6%] How many cycles are required to complete the code segment, if you have no forwarding path? And, how many cycles are required to complete the code, if you have implemented necessary

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forwarding paths.

(3) [2%] Try to reorder the code sequence to avoid stalls. Please write down the new code sequence.

七. [25%] Please design a GCD (Greatest Common Divisor) calculator to calculate two numbers kept in registers (says R0 and R1), and place the result in the third register (says R2).

(1) [7%] Define the types and formats of instructions required for your GCD calculator. Explain the instruction formats you defined.

(2) [7%] Implement the GCD calculator with the assembly instructions you defined in (a).

(3) [7%] Implement all the instructions you defined in (a) using the basic building blocks (register file, memory, ALU, adder, MUX, etc).

(4) [4%] Continuing on (c), illustrate the datapath of your GCD calculator.

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