國立中央大學 109 學年度碩士班考試入學試題

所別： 資工類

科目： 作業系統與計算機組織

本科考試禁用計算器 ＊請在答案卷(卡)內作答

單選題（每選項單獨計分，每題 5 分，答錯倒扣 2 分）倒扣到該大題 0 分為止

1. Assume that an un-pipelined machine has 9ns clock cycles. The machine uses 4 cycles for ALU operations, 5 cycles for branches, and 5 cycles for memory operations. The relative frequencies of these operations are 30%, 30%, and 40%, respectively. Suppose that pipelining the machines adds 1ns of overhead to the clock cycle time. Assume that the ideal CPI is one. Ignore any other impact.
   (A) 4.5
   (B) 4.6
   (C) 4.7
   (D) 4.8
   (E) 4.9

2. For a 4K-byte direct-mapped cache whose block size is 4 bytes, if the length of the address is 32 bits, how many bits are used for tag?
   (A) 18
   (B) 19
   (C) 20
   (D) 21
   (E) 22

多選題 (每選項單獨計分，每題 5 分，每答對一個選項得一分，答錯一個選項倒扣一分) 倒扣到該大題 0 分為止

3. Which of the following instructions should be sensitive in a VM executes native instructions ?
   (A) Set value of timer.
   (B) Read the clock.
   (C) Clear memory.
   (D) Issue a trap instruction.
   (E) Disable interrupts.

4. Which of the following scheduling algorithms would result in starvation?
   (A) First-come, first-served
   (B) Shortest job first
   (C) Round robin
   (D) Priority
   (E) Weighted fair queueing

參考用

注意:背面有試題

國立中央大學 109 學年度碩士班考試入學試題

5. A counting semaphore ____.
   (A) is essentially an integer variable
   (B) is accessed through only one standard operation
   (C) can be modified simultaneously by multiple threads
   (D) cannot be used to control access to a thread's critical sections
   (E) executes as a single, uninterruptible unit

6. Consider a multiprocessor system and a multithreaded program written using the many-to-many threading model. Let the number of user-level threads in the program be more than the number of processors in the system. What are the lower performance implications of the following scenarios.
   (A) The number of kernel threads allocated to the program is less than the number of processors.
   (B) The number of kernel threads allocated to the program is equal to the number of processors.
   (C) The number of kernel threads allocated to the program is greater than the number of processors but less than the number of userlevel threads.
   (D) The number of kernel threads allocated to the program is equal to two.
   (E) The number of kernel threads allocated to the program is greater than the number of processors and also greater than the number of userlevel threads.

7. Consider the following page reference string:
   7, 2, 3, 1, 2, 5, 3, 4, 6, 7, 1, 0, 5, 4, 6, 2, 3, 2, 3, 0 , 1.
   Assuming demand paging with three frames, how many page faults would occur for the following replacement algorithms?
   • LRU replacement
   • FIFO replacement
   • Optimal replacement
   Select the correct answers:
   (A) 18 for LRU
   (B) 19 for FIFO
   (C) 17 for FIFO
   (D) 14 for LRU
   (E) 14 for optimal replacement

8. When using computers, normal users are generally not actively aware of
   (A) Resource allocation
   (B) Interactivity
   (C) Continuity

國立中央大學 109 學年度碩士班考試入學試題

所別： 資工類 共6頁 第3頁

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(D) Responsiveness
(E) None of the above

9. Choose the correct statements from the multiple choices
   (A) TLBs are more beneficial with multi-level page tables than with single-level page tables.
   (B) Given a constant number of bits in a virtual address, the size of a linear page table decreases with larger pages.
   (C) The longer the time slice, the more a RR scheduler gives similar results to a FIFO scheduler.
   (D) An SJF scheduler may preempt the currently running job.
   (E) None of the above.

10. Choose the correct statements from the multiple choices
   (A) Multiprogramming is unnecessary on single-user systems
   (B) When an I/O operation completes, the previously blocked process moves into the RUNNING state.
   (C) If a physical address is 32 bits and each page is 4KB, the top 18 bits exactly designate the physical page number.
   (D) The number of virtual pages is identical to the number of physical pages.
   (E) None of the above

11. Choose the correct statements from the multiple choices
   (A) Given a 2-level page table (and no TLB), exactly 3 memory accesses are needed to fetch an instruction
   (B) In an unsafe state, the operating system is deadlocked.
   (C) Banker's algorithm is a deadlock avoidance algorithm.
   (D) The wait-for graph is used for deadlock detection.
   (E) None of the above.

12. Choose the correct statements from the multiple choices regarding networking.
   (A) The length of IPv6 header is four times the length of IPv4 header.
   (B) IPv6 does not support broadcast address type.
   (C) IPsec security is mandated in the IPv6 protocol specification.
   (D) IPv6 does not allow routers to fragment packets.
   (E) None of the above.

參考用

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13. About single-cycle and multi-cycle implementation of CPU in computer organization, which of the following statements are NOT true?
    (A) Single-cycle implementation of CPU is not used in the mainstream processors nowadays.
    (B) For single-cycle implementation of CPU, the clock cycle is determined by the shortest possible path.
    (C) Single-cycle implementation of CPU allows a functional unit to be used more than once per instruction.
    (D) Compared to single-cycle implementation, multicycle implementation is more efficient.
    (E) Multicycle implementation is more suitable for pipeline implementation.

14. Which of the following statements are NOT true?
    (A) For a cache with write back strategy, read misses might result in writes.
    (B) For a cache with write through strategy, a write buffer is not necessary.
    (C) Write after write (WAW) hazards can be resolved by register renaming.
    (D) Read after write (RAW) hazards can be resolved by register renaming.
    (E) Distributed shared-memory scheme will not result in non-uniform memory access time for multiprocessor machines.

15. Which of the following statements are true?
    (A) The motivation of dynamic scheduling does not include preventing out-of-order completion.
    (B) Using separated instruction cache and data cache instead of a unified cache could mainly reduce data hazard.
    (C) Reduced instruction set computer (RISC) has become obsolete now.
    (D) Long memory latency and limits of power have limited the growth of uniprocessor performance and motived the trend of developing multiple processors per chip in recent years.
    (E) None of the above

16. Which of the following statements are true regarding virtual memory?
    (A) Address translation is a process to translate a virtual address to register number.
    (B) Physical address is an address of the register

(C) If translation-lookaside buffer (TLB) misses, it is possible to find the entry in page table.
(D) The number of bits for the virtual page number in virtual address has to be the same as the number of bits for the physical page number in physical address.
(E) When an OS performs context switch from P1 to P2, the OS must ensure P2 cannot get access to the page tables of P1.

17. Which of the following statements are true regarding the design of a MIPS CPU?
(A) Data forwarding can be used to partially solve Read-After-Write hazard.
(B) Branch prediction helps prevent data hazard.
(C) Pipelining reduces the time it takes to complete an individual instruction.
(D) The branch target address of the beq instruction is known at the compile time.
(E) Pipelining increases the number of simultaneously executing instructions.

18. Which of the following statements are true regarding MIPS ISA?
(A) The stack frame is the collection of all data on the stack associated with one subprogram call.
(B) The frame pointer is a register that stores the address to the top of the stack.
(C) Stack overflow happens when the stack pointer exceeds the stack bound.
(D) The jal instruction should be called when a procedure finishes and ready to return to the caller.
(E) The beq instruction has three operands: two registers that are compared for equality, and a register to specify the branch target address.

19. Which of the following statements are true regarding memory and cache?
(A) Spatial locality means that if an item is referenced, it will tend to be referenced soon.
(B) Increasing the size of a cache block makes better use of the spatial locality.
(C) If we use the "write through" policy, the dirty bit is needed.
(D) When increasing cache associativity, we increase the utilization of the cache
(E) A direct mapped cache has a lower cache miss rate than a fully associative cache.

20. Which of the following statements are true regarding pipelining and parallelization?
(A) The purpose of loop unrolling is to decrease program code size.

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(B) The purpose of register renaming is to increase readability.
(C) The VLIW (Very Long Instruction Word) is a style of instruction set architecture that launches many dependent operations in a single wide instruction.
(D) A superscalar processor can dispatch multiple instructions simultaneously.
(E) The static multiple issue is an approach to implement a multiple-issue processor where many decisions are made by the compiler.