

國立中央大學 110 學年度碩士班考試入學試題

所別： 資工類

共 5 頁 第 1 頁

科目： 作業系統與計算機組織

本科考試禁用計算器

*請在答案卷(卡)內作答

多選題（每題五分，每個選項單獨計分，答錯一個選項倒扣一分，倒扣至多選題 0 分為止）

1. Given (1) an instruction has 32 bits, and (2) a cache memory with 64 blocks, 16 bytes/block, and 4-way set associative. Which of the following statements are true?
 - a. Byte address 1200 maps to the set number 11
 - b. The index field requires 4 bits
 - c. The offset field is 12 bits
 - d. The tag field is 16 bits
 - e. None of the above
2. Which of the following statements are true for memory hierarchy?
 - a. Spatial locality refers to the situation that an item tends to be referenced soon once it is referenced.
 - b. When increasing the size of a cache block, the miss penalty decreases
 - c. Increasing cache associativity decreases the utilization of a cache
 - d. A valid bit indicates whether the data in a block is valid or not
 - e. A cache block is the basic unit for the cache storage
3. Which of the following statements are true regarding the pipeline hazards of a 5-stage MIPS CPU?
 - a. The data forwarding technique passes data to the previous instructions that need the data
 - b. The structural hazard happens when a required resource is busy
 - c. Rearranging the instructions may solve some of the data hazards
 - d. If we put the register comparator and the target address calculator at the ID stage, then 2 stalls are needed for a branch hazard
 - e. If we put the register comparator and the target address calculator at the ID stage, and a comparison register is a destination of immediately preceding load instruction, then 1 stall is needed
4. Given the execution time of the 5 stages of a CPU: IF 200 ps, ID 100 ps, EXE 200 ps, MEM 200 ps, WB 100 ps, which of the following statements are true?
 - a. The ideal cycle time of a single cycle CPU is 800 ps
 - b. The ideal execution time of "sw" for a single cycle CPU is 800 ps
 - c. The ideal cycle time of a multiple cycle CPU is 200 ps
 - d. The ideal execution time of "lw" for a multiple cycle CPU is 800 ps
 - e. None of the above

注意:背面有試題

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共 5 頁 第 2 頁

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5. Given a 16-bit computer with the I-type instruction in the following format, which of the following statements are true?

op: 5 bits	rs: 3 bits	rt: 3 bits	immediate: 5 bits
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- a. The computer supports at most 16 operations
 - b. The computer has 8 registers
 - c. The range of the number in the immediate field (in 2's complement) is from -2^5 to $2^5 - 1$
 - d. Each register is 8-bits long
 - e. None of the above
6. Which of the following statements are true for dynamic branch prediction?
- a. Branch history table or branch prediction buffer can be implemented as a memory indexed by the lower bits of the program counter address.
 - b. Branch prediction buffer must have tag and address check.
 - c. A 2-bit dynamic branch predictor must miss twice before the prediction is changed.
 - d. Mis-prediction can be caused by getting the branch history of wrong branch when indexing the branch history table.
 - e. Correlating branch predictors assume that the behaviour of a branch would not be affected by the behaviours of other branches.
7. For RISC (Reduced Instruction Set Computer), which of the following statements are true?
- a. For any given level of general performance, a RISC chip will typically have far more transistors dedicated to the core logic compared with CISC (complex instruction set computer).
 - b. RISC allows designers to increase the size of the register set.
 - c. RISC usually uses uniform instruction format with the opcode in the same bit positions in every instruction, which demands less decoding complexity.
 - d. RISC is not suitable for pipeline design and would decrease internal parallelism.
 - e. RISC usually supports more addressing modes than CISC.
8. Assume that the frequency of Floating Point (FP) operations is 25% for a computer, and the average CPI (Clock Cycles Per Instruction) of FP operations is 4. The average CPI of other instructions is 1.5. By performing some enhancement on the hardware, we can reduce the average CPI of all FP operations to 2. All other factors are not changed after enhancement. Which of the followings are true?

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共 5 頁 第 3 頁

科目： 作業系統與計算機組織

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- a. The speedup for the FP operations is 2
- b. The total speedup can be computed by Amdahl's Law using the following equation:

$$speedup = \frac{1}{(1-0.25) + \frac{0.25}{2}} = 1.1428$$

- c. The total speedup is 1.307
- d. The CPI after enhancement is 1.859
- e. The CPI before enhancement is 2.125

9. About instruction level parallelism, which of the followings are true?

- a. To perform loop unrolling, loop iterations must be independent with no loop-carried dependence.
- b. True dependencies can be resolved by register renaming.
- c. Anti-dependence occurs when instruction j writes a register or memory location that instruction i read from, and instruction i is executed first.
- d. Loop unrolling can reduce control stalls.
- e. Issuing multiple instructions per cycle can not reduce ideal CPI.

10. About memory hierarchy, which of the followings are true?

- a. For virtual memory, usually write-through strategy is used to update the lower level storage.
- b. Implementing higher associativity in cache can reduce conflict miss.
- c. For virtual memory, usually fully associative placement strategy is used.
- d. If the page size is larger, the size of the page table is also larger.
- e. If write-back strategy is used, it is possible that read misses would produce writes.

複選題-第十一題到第二十題為複選題（全對才給分）：每一題答對給 5 分、答錯不倒扣。

11. What are the factors that should be considered when deciding the page size?

- a. Size of page table
- b. Fragmentation
- c. I/O overhead
- d. Number of page faults
- e. None of the above

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12. Choose the correct statements from the multiple choices regarding threads
- a. Kernel-level threads are easier and faster to create than user-level threads
 - b. Different user-level threads of the same process can have different scheduling priorities
 - c. A blocking kernel-level thread blocks all threads in the process
 - d. For the Many-to-One multithreading model, one thread blocking causes all to block
 - e. None of the above
13. Choose the correct statements from the multiple choices regarding deadlocks
- a. If the resource allocation graph contains a cycle, then the system is deadlocked
 - b. If a system is in an unsafe state, then there is no allocation sequence that allows the processes to finish executing
 - c. Pretending that deadlocks never occur in the system is a method to deal with deadlocks
 - d. Banker's algorithm is a deadlock prevention algorithm
 - e. None of the above
14. Choose the correct statements from the multiple choices
- a. Each **container** includes the application, the necessary binaries and libraries and an entire guest operating system
 - b. Containers running on a single machine all share the same operating system kernel
 - c. Virtual machine run as an isolated process in user space on the host operating system
 - d. Containers are **lightweight than virtual machines**
 - e. None of the above
15. Choose the correct statements from the multiple choices
- a. It is not allowed for routers to fragment IPv6 packets.
 - b. DHCP allows a host to dynamically obtain its IP address from network server when it joins the network.
 - c. NAT is used to translate IP addresses to hardware addresses.
 - d. DNS is used to find the hardware address of a local device
 - e. None of the above

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16. When communicating with sockets, a client process initiates a request for a connection and is assigned a port by the host computer. Which of the following would be a valid port assignment for the host computer?
- 21
 - 23
 - 80
 - 1625
 - None of the above
17. _____ is/are not a technique/s for handling critical sections in operating systems.
- Nonpreemptive kernels
 - Preemptive kernels
 - Spinlocks
 - Peterson's solution
 - Dekker's algorithm
18. Assume a system has a TLB hit ratio of 90%. It requires 15 nanoseconds to access the TLB, and 85 nanoseconds to access main memory. What is the effective memory access time in nanoseconds for this system?
- 108.5
 - 100
 - 22
 - 176.5
 - 32
19. Given the reference string of page accesses: 1 2 3 4 2 3 4 1 2 1 1 3 1 4 and a system with three page frames, what is the final configuration of the three frames after the LRU algorithm is applied? Assume the FIFO queue is left out right in.
- 1, 3, 4
 - 3, 1, 4
 - 4, 1, 2
 - 1, 2, 3
 - 1, 4, 3
20. Which of the following is true of a blocking system call?
- The application continues to execute its code when the call is issued.
 - The call returns immediately without waiting for the I/O to complete.
 - The execution of the application is suspended when the call is issued.
 - Blocking application code is harder to understand than nonblocking application code
 - None of the above

