國立中央大學 112 學年度碩士班考試入學試題

所別： 資工類

科目： 作業系統與計算機組織

多選題 (每題 5 分，共 20 題，答錯每個選項倒扣 1 分)

1. Which of the following statements are true regarding performance evaluation?
   A. Throughput refers to the time a system takes to process a request after receiving it.
   B. If a CPU's clock rate is an integer, its cycles per instruction (CPI) must also be an integer.
   C. If a component accounts for 30% of the total execution and we shrink the execution time of this component to half, the total execution time becomes 85% of the original execution time.
   D. In a multi-threading environment, CPU time could be higher than the elapsed time.
   E. None of the above.

2. Which statements are true about segmentation fault? The code segments are written in C.
   A. Segmentation fault happens when a program attempts to access memory in the heap segment.
   B. Executing the following code may cause a segmentation fault.
   ```
   char* p = NULL; printf("%c\n", *p);
   ```
   C. Executing the following code may cause a segmentation fault.
   ```
   char* p; printf("%c\n", *p);
   ```
   D. Executing the following code may cause a segmentation fault.
   ```
   int foo() {return foo();}
   ```
   E. None of the above.

3. Which statements are true about the MIPS (32-bit) assembly language?
   A. The I-type instructions are composed of the OP code (6 bits), RS (5 bits), RT (5 bits), and constant field (16 bits). Therefore, an I-type instruction can take at most two registers.
   B. The instruction JUMP comprises the OP code (6 bits) and the address field (26 bits). Therefore, a JUMP instruction can jump to 2^{26+2} bytes before or after the address specified by the stack pointer (SP) register.

注意:背面有試題

C. The JR (jump register) instruction causes the PC to jump to the content of a register. Therefore, JR is a J-type instruction.

D. The logic of "logical-shift-left" and "arithmetic-shift-left" operations are different. Therefore, MIPS needs to provide instructions for each of them.

E. None of the above.

4. Which statements are true about single-cycle, multi-cycle, and pipeline CPUs?

A. The pipeline structure reduces the response time for each instruction.

B. You are given a program with 10 instructions. If you can perfectly pipeline each instruction into 5 stages with no bubbles (and each stage takes 1 ns), it takes 14 ns to complete the 10 instructions.

C. A multi-cycle CPU is better than a single-cycle CPU because a multi-cycle CPU tends to have a lower value of CPI (cycles per instruction).

D. With more pipeline stages, the performance is less likely to be influenced by hazards.

E. None of the above

5. Which of the following statements are true about RISC and CISC?

A. The execution time of a RISC instruction is usually faster than a CISC instruction

B. CISC usually has a more uniform instruction format than RISC.

C. RISC is an outdated technology.

D. RISC uses a simpler instruction set than CISC.

E. None of the above.

6. Which of the following statements are true about RAM and ROM?

A. RAM can be randomly read and written.

B. ROM can be read and written.

C. RAM cannot be persistent storage because of its volatility.

D. ROM can persistently preserve program.

E. All of the above

所別： 資工類

科目： 作業系統與計算機組織

7. Which of the following statements are true about cache design?
   A. In an inclusive cache design, the top-level cache (e.g., L1 cache) is the subset of the bottom-level cache (e.g., L2 cache).
   B. Because the first-level cache needs a short hit time, the size of the first-level cache is big.
   C. Reducing the miss penalty can decrease average memory access time when the top-level cache's hit time is smaller than the bottom-level cache's hit time.
   D. Generally, the full-associative cache design has lower cache hit rate than the direct-mapped cache design.
   E. None of the above.

8. Which of the following statement are true about cache miss types?
   A. Compulsory misses can be avoided by a prefetching mechanism.
   B. Conflict miss occurs the first time a location is used.
   C. Capacity miss occurs when other external processors update data.
   D. Direct-mapped cache has more conflict misses than n-way associative caches (where n > 1).
   E. All of the above

9. Suppose that a cache memory's (L1) access time is "*C* ns" and a main memory's (L2) access time is "*M* ns". In this architecture, 60% of the memory accesses are read and remaining all are writing requests. If the hit ratio of read operation can achieves "*H*" and that of writing operation is 1, what is the average memory access time (AMAT) when a write-through protocol is adopted on the cache?
   A. M (0.6H + 1) + 0.6HC
   B. 0.6 (H + C + M)
   C. 0.6H (C + M) + M
   D. 0.6H + 0.6(C + M)
   E. None of the above

所別： 資工類

科目： 作業系統與計算機組織

10. If the floating-point (FP) instructions of an application on a specific processor ***C1*** consumes 60% of the total execution time. Moreover, in the same application, 25% of the floating-point time is taken to do square root calculations. A new processor ***C2*** is developed. This new processor could either enhance the performance of FP instructions by a factor of 1.5 or alternatively increase the performance of the square root operation by a factor of 8. Which of the following statements are true?
    A. Enhancing the performance of FP instruction by a factor 1.5 is **worse** than increasing the performance of the square root operation by a factor of 8.
    B. Enhancing the performance of FP instruction by a factor 1.5 is **better** than increasing the performance of the square root operation by a factor of 8.
    C. The speed-up of the FP instruction enhancement is 1.25.
    D. The speed-up of the square root operation enhancement is 1.15.
    E. None of the above.

11. Choose the correct statements from the multiple choices
    A. Deadlock can be avoided by using a deadlock detection algorithm.
    B. A user-level process cannot modify its own page table entries
    C. Shortest Remaining Time First is the best preemptive scheduling algorithm that can be implemented in an Operating System.
    D. When a process is created using the classical fork() system call, process ID is inherited by the child process
    E. None of the above

12. Choose the correct statements from the multiple choices regarding pipes
    A. Ordinary pipes are unidirectional, allowing only one-way communication.
    B. The system call pipe() provides reliable, bidirectional communication between processes on the same host.
    C. If two-way communication is required, two named pipes must be used with each pipe sending data in a different direction.
    D. Only byte-oriented data may be transmitted across a UNIX FIFO.
    E. None of the above

注意:背面有試題

所別： 資工類

科目： 作業系統與計算機組織

13. Choose the correct statements from the multiple choices regarding networking technologies
    A. The goal of Web 3.0 is to enable a more decentralized internet.
    B. The architecture of software-defined networking is decentralized.
    C. The Domain Name System is a distributed, hierarchical database.
    D. Internet standards are developed by the Internet Engineering Task Force.
    E. None of the above

14. Choose the correct statements from the multiple choices
    A. A process can move form a ready state to the waiting state.
    B. The reference bit is set by the hardware.
    C. The mode bit provides ability to identify in which particular mode the current instruction is executing.
    D. If the valid-invalid bit for a page is set, it is required to write the memory page to the disk for page replacement.
    E. None of the above

15. Choose the correct statements from the multiple choices
    A. The copy-on-write technique allows the parent and child processes initially to share the same pages.
    B. No parent-child relationship is required for named pipes.
    C. IPSec can be used to setup virtual private networks.
    D. The race condition can be solved by the banker's algorithm.
    E. None of the above

16. Identify the following environments need hard real-time scheduling.
    A. Thermostat in a household.
    B. Control system for a nuclear power plant.
    C. Fuel economy system in an automobile.
    D. Landing system in a jet airliner.
    E. Mailing system.

注意:背面有試題

17. Which of the following scheduling algorithms would result in starvation?
    A. First-come, first-served
    B. Shortest job first
    C. Round robin
    D. Priority
    E. Weighted fair queueing

18. A counting semaphore ____.
    A. is essentially an integer variable
    B. is accessed through only one standard operation
    C. can be modified simultaneously by multiple threads
    D. cannot be used to control access to a thread's critical sections
    E. executes as a single, uninterruptible unit

19. Consider a multiprocessor system and a multithreaded program written using the many-to-many threading model. Let the number of user-level threads in the program be more than the number of processors in the system. What are the lower performance implications of the following scenarios?
    A. The number of kernel threads allocated to the program is less than the number of processors.
    B. The number of kernel threads allocated to the program is equal to the number of processors.
    C. The number of kernel threads allocated to the program is greater than the number of processors but less than the number of userlevel threads.
    D. The number of kernel threads allocated to the program is equal to two.
    E. The number of kernel threads allocated to the program is greater than the number of processors and also greater than the number of userlevel threads.

所別： 資工類

科目： 作業系統與計算機組織

20. Some computer systems do not provide a privileged mode of operation in hardware. To construct a secure operating system for these computer systems, an OS for a machine of this type would need to remain in control at all times. This is could be accomplished by the following methods:
    A. software interpretation of all user programs.
    B. co-execution with co-processor to execute all programs.
    C. networked server support to execute programs.
    D. all programs be written in high-level languages so that all object code is compiler produced and checked.
    E. cluster computing in database cloud system.