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多選題(每一選項單獨計分,不倒扣)

- 1. (5 pts.) Which of the following statements are true about the assumption and definition of branch prediction?
 - (A) Data that is being operated on has regularities.
 - (B) Underlying algorithm has regularities.
 - (C) Static branch prediction usually outperforms dynamic branch prediction.
 - (D) The hypothesis of correlating branches is that the behavior of other branch instructions do not affect the prediction of current branch.
 - (E) In general, an (m, n) correlating predictor records the last m branches to select between m history tables each with n-bit counters.
- (5 pts.) Suppose that FPSQR instructions are improved with speedup=10. FPSQR instructions are responsible for 20% of the execution time. What is the overall speedup?
 (A) 1.08
 (B) 1.22
 (C) 1.35
 (D) 1.55
 (E) 1.67
- 3. (5 pts.) Compute the clock cycle per instruction (CPI) for the following instruction mix. The mix includes 22% loads, 11% stores, 49% R-format operations, 16% branches, and 2% jumps. The number of clock cycles for each instruction class is listed as follows. 5 cycles for loads, 4 cycles for stores, 4 cycles for R-format instructions, 3 cycles for branches, 3 cycles for jumps.
 - (A) 3.58 (B) 3.76 (C) 4.04 (D) 4.28 (E) 4.52
- 4. (5 pts.) Which of the following statements are true?
 - (A) RISC architecture usually needs more special purpose registers than CISC.
 - (B) For a cache with write back strategy, read misses might result in writes.
 - (C) The advantages of dynamic scheduling include memory latency hiding and resolving real dependence which is unknown at compile time.
 - (D) Out-of-order completion might result in write after write (WAW) and write after read (WAR) hazards.
 - (E) Distributed shared-memory scheme might result in non-uniform memory access time for multiprocessor machines.
- 5. (5 pts.) What is the average memory access time for the memory with the following two-way set-associative cache? The hit time is 1.1 clock cycle. The miss rate is 0.04. And the miss penalty is 8 clock cycles.

參考用

注:背面有試題

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- (A) 1.02 clock cycles (B) 1.12 clock cycles (C) 1.22 clock cycles
- (D) 1.32 clock cycles (E) 1.42 clock cycles
- 6. (5 pts.) K is the 32-bit IEEE754 floating-point number of (1987/6). N is the number of bits equal to '1' in K. What is "N mod 5"?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

- 7. (5 pts.) Which of the following statement(s) are correct?
 - (A) Inserting L2 cache will not affect the miss rate of L1 cache.
 - (B) The case of "TLB hit, Page Table hit, Cache miss" is possible.
 - (C) One of the advantages of the superscalar processor over VLIW is the backward compatibility of the software.
 - (D) In a pipelined system, forwarding can help to eliminate all the stalls resulting from data hazards.
 - (E) The advantage of using microprogramming in designing the control is the execution speed.
- 8. (5 pts.) Which of the following sum terms must be included in the sum-of-products simplification for (A'+B+C')(A+C+D')(A+B+C)(B+D)
 (A) AB (B) BD' (C) A'BD (D) AC'D (E) A'CD
- 9. (5 pts.) A 32-bit cache memory address is decomposed into 3 fields as :

| 31 | 19 18 | 4.3 0 |
|-----|-------|--------|
| Tag | Set | Offset |

Assume the cache is 2-way set associative. The total size (including tag and data bits but excluding other valid/dirty bits) of the cache memory is L KB(Kbytes). N=round(L) mod 5. Then N is equal to (A) 0 (B) 1 (C) 2 (D) 3 (E) 4

10. (5 pts.) We want to evaluate the performances of two computers M1 and M2. M1 has a clock rate of 1GHz and M2 has a clock rate of 800MHz. The following shows the CPI of 3 instruction classes:

| Instruction Class | CPI for M1 | CPI for M2 | |
|-------------------|------------|------------|--|
| A | 3 | 2 | |
| В | 4 | 4 | |
| С | 4 | 3 | |

There are 3 compilers: C1, C2, C3 that produce the instruction mixes as follows:

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| Instruction Class | C1 | C2 | C3 |
|-------------------|-----|-----|-----|
| A_{i} | 30% | 25% | 50% |
| В | 50% | 25% | 30% |
| С | 20% | 50% | 20% |

Assume that any of the three compilers (C1, C2, C3) can be used in M1 and M2. We also assume that the numbers of instructions from C1 and C2 are the same for both M1 and M2 and equal to 1000, while the number of instructions from C3 is 1050 (for both M1 and M2). Which of the following combinations of compiler + computer will you choose?

- (A) C1+M1 (B) C2+M1 (C) C3+M1 (D) C2+M2 (E) C3+M2
- 11. (5 pts.) Most systems allow programs to allocate more memory to its address space during execution. Data allocated in the heap segments of programs is an example of such allocated memory. What is required to support dynamic memory allocation in the following schemes:
 - (A) contiguous-memory allocation. (B) pure segmentation. (C) pure paging. (D)paged segmentation (E)none
- 12. (5 pts.) Consider a demand-paging system with the following time-measured utilizations: CPU utilization 20%, Paging disk 97.7%, Other I/O devices 5%. Which (if any) of the following will (probably) improve CPU utilization?
 - (A) Install a faster CPU.
 - (B) Install a bigger paging disk.
 - (C) Increase the degree of multiprogramming.
 - (D) Decrease the degree of multiprogramming.
 - (E) Install more main memory.
- 13. (5 pts.) Which of the functionalities listed below need to be supported by the operating system for the real-time systems?
 - (A) Batch programming
 - (B) Virtual memory
 - (C) Time sharing
 - (D) Spooling
 - (E) Interrupt driving
- 14. (5 pts.) What are the purposes of the separation of mechanism and policy?
 - (A) Easy for programming

生:背面有試題



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- (B) Systems are easy to modify
- (C) Flexibility to suit its needs
- (D) Increasing utilization
- (E) Quick and fast system response
- 15. (5 pts.) For a graphics card with direct bus connection accessible through memory mapped I/O, the better designs of the operating system are to use (A)buffering, (B)spooling, (C)caching, and (D)polled I/O or interrupt-driven I/O, (E) neither of polled I/O and interrupt-driven I/O.
- 16. (5 pts.) Which of the following scheduling algorithms could not result in starvation?
 - (A) First-come, first-served
 - (B) Shortest job first
 - (C) Round robin
 - (D) Priority
 - (E) None
- 17. (5 pts.) Choose the correct statements from the multiple choices regarding the real-time scheduling of Linux.
 - (A) Linux's real-time scheduling is soft-real time.
 - (B) Linux's kernel can guarantee a minum latency between when a process becomes runnable and when it actually runs.
 - (C) Linux's scheduler offers strict guarantees about the relative priorities of real-time process.
 - (D) Linux implements both First Come, First Served (FCFS) and Round-Robin (RR) real-time scheduling classes.
 - (E) Among processes of equal priority, Linux will run process randomly.
- 18. (5 pts.) Choose the correct statements from the multiple choices regarding the disk scheduling.
 - (A) The SCAN scheduling performs better for systems that place a heavy load on the disk.
 - (B) Either SSTF or LOOK is a reasonable choice for the default algorithm.
 - (C) Solid-State Drives (SSD) commonly use an FCFS policy.
 - (D) The Linux Noop scheduler uses an FCFS policy.
 - (E) None of the above.



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- 19. (5 pts.) Choose the correct statements from the multiple choices regarding cloud computing.
 - (A) Software as a service (SaaS) provides a software stack ready for application use via the Internet.
 - (B) SaaS is a software delivery model in which software and associated data are centrally hosted on the cloud.
 - (C) SaaS provides one or more applications available via the Internet.
 - (D) A database server is a kind of SaaS.
 - (E) None of the above
- 20. (5 pts.) Choose the correct statements from the multiple choices.
 - (A) The subnet mask for the subnet 200.23.16.0/23 is 255.255.255.0.
 - (B) The subnet 200.23.16.0/23 could accommodate up to 256 hosts.
 - (C) The broadcast address of the subnet 192.168.5.0/26 is 192.168.5.255.
 - (D) The number of available subnets for a /26 network is 8.
 - (E) None of the above.

