

# 國立中央大學九十學年度碩士班研究生入學試題卷

所別: 電機工程學系 甲、乙組 科目: 電子學 共 2 頁 第 1 頁

1. (15%)

Consider the BiCMOS circuit shown in Fig. 1. The bias voltage  $V_B$  is adjusted for a dc output voltage of 2 V and  $R_B = 1 \text{ K}\Omega$ . The transistor parameters are:  $\mu_n C_{ox} = 60 \mu\text{A}/\text{V}^2$ ,  $W = 40 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ , and  $V_{TH} = 0.8 \text{ V}$  for MOSFET, and  $I_S = 10^{-16} \text{ A}$ ,  $\beta_F = 100$ .

- Calculate the bias currents in both transistors,  $I_{D1}$  and  $I_{C1}$ .
- Calculate the small-signal voltage gain  $v_o/v_i$ .
- Find out the output resistance  $R_o$ .

2. (15%)

If the Early voltage  $V_A = 100 \text{ V}$  and the common-emitter current gain  $100 < \beta_F \leq 180$ ,  $V_{BE(on)} = 0.7 \text{ V}$

- Please design the emitter-follower circuit (Fig. 2) (choose the appropriate values of  $R_1$ ,  $R_2$  and  $\beta_F$ ) such that the minimum current gain  $A_i = i_o/i_s = 10$ .
- The input signal source is given by  $v_s = V_m \sin \omega_o t$ , determine the maximum value of  $V_m$  that will produce a symmetrical sinusoidal output signal.

3. (25%)

Consider the circuit shown in Fig 3, assume MOSFETs are operating in saturation region and BJTs are operating in forward active region,  $\mu_n C_{ox} W/L = 25 \text{ mA}/\text{V}^2$  for all MOSFETs,  $\beta = 100$  for all BJTs,  $V_T = 25 \text{ mV}$ ,  $C_\pi = C_{gs} = 0.5 C_{L2} \ll C_{L1}$  and  $C_\mu = C_{gd} \ll C_{L2}$ , neglect  $r_o$ ,  $C_{cs}$  and  $C_{ds}$ .

(5%) (a) The small signal DC gain of amplifier 3.a and 3.b are  $A_1$  and  $A_2$  respectively, which statement is correct? (1)  $A_1 > A_2$  (2)  $A_1 < A_2$  (3)  $A_1 = A_2$  (答錯倒扣 2%)

(5%) (b) The phase margin of amplifier 3.a and 3.b are  $\phi_1$  and  $\phi_2$  respectively,  $\phi_2 = 60^\circ$ , which statement is correct? (1)  $\phi_1 > \phi_2$  (2)  $\phi_1 < \phi_2$  (3)  $\phi_1 = \phi_2$  (答錯倒扣 2%)

(15%)(c) Assume amplifier 3.b has a 3dB bandwidth of 10kHz and a phase margin of  $60^\circ$ , inverting amplifier Ax has a 3dB bandwidth of 600 MHz and a small signal DC gain of -4, neglect the loading effect of Ax, what is the resulting 3dB bandwidth (5%) and phase margin (10%) of amplifier 3.c.

4. (15%)

Consider the circuit shown in Fig 4, assume  $V_T = 25 \text{ mV}$  and  $\beta = 100$  for Q1-Q4. (a) What kind of feedback topology (shunt-shunt, series-shunt, shunt-series, series-series) is utilized in this amplifier? (5%)

(b) Small signal DC gain  $V_o/V_i = ?$  (10%)

5. (15%)

In the CMOS bistable circuit shown, all transistors have  $|V_t| = 1 \text{ V}$  and, with  $k = 1/2 k' (W/L)$ ,  $k_1 = k_2 = k_3 = k_4 = 2k_5 = 2k_6 = 200 \mu\text{A}/\text{V}^2$ , (a) Sketch and label the voltage transfer characteristic of the Q3-Q4 inverter. (5%)

請用

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(b) Sketch and label the transfer characteristic  $V_o$  versus  $V_i$ . (5%)

(c) Find the  $V_{IH}$  and  $V_{IL}$ . (5%)

6 (15%)

A particular two-input NOR gate has  $t_{PHL} = 1$  ns and  $t_{PLH} = 3$  ns. Five such gates, each with one input low, are connected in cascade to form a ring.

(a) Find the oscillation frequency. (5%)

(b) Two additional such gates, A and B, are connected to the ring, gate A inputs to the outputs of gates 1 and 3, and gate B inputs to the outputs of gates 1 and 4. Sketch and label the waveforms at all NOR gate outputs. (10%)

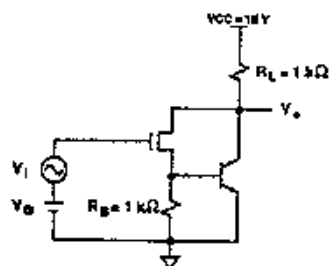


Fig 1/ Problem 1

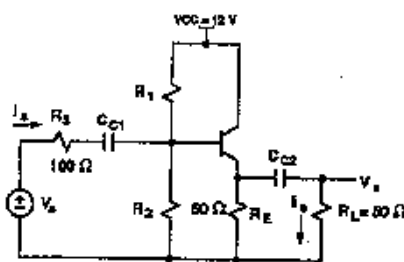


Fig 2/ Problem 2

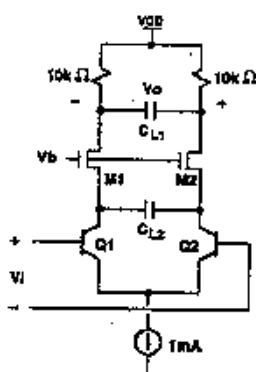


Fig 3.a/ Problem 3

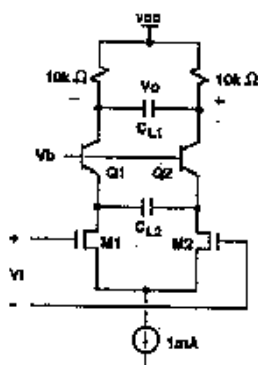


Fig 3.b/ Problem 3

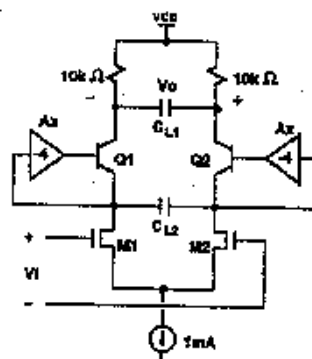


Fig 3.c/ Problem 3

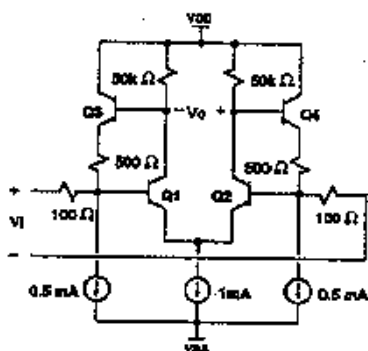


Fig 4/ Problem 4

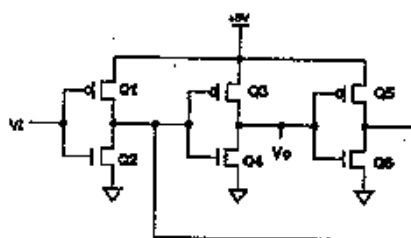


Fig 5/ Problem 5