國立中央大學九十學年度碩士班研究生入學試題卷

所別: 電機工程學系 甲組 科目: 數位系統 共 1 頁 第 1 頁

(25%)
For $f(A,B,C) = \sum m(0,2,3,5,7)$ use the following methods to implement the circuit. Assume that both the positives (A, B, C) and the negatives ($\overline{A},\overline{B},\overline{C}$) of the inputs are available.

(a) Use only two-level NAND-gate network (5%)
(b) Use only two-level NOR-gate network. (5%)
(c) Use an active high 3-to-8 decoder and a NOR gate of any number of inputs. (A, B, C) are connected to (S2, S1, S0) respectively. (7%)
(d) Use a 4-to-1 MUX with A connected to S1 and B to S0. (8%)

(25%)
For $f(A,B,C,D) = A\overline{C}\overline{D} + \overline{A}\overline{B}C + AC\overline{D} + BCD + \overline{A}B\overline{C} + \overline{A}\overline{B}\overline{D}$

(a) Draw the K-Map (5%)
(b) List all the prime implicants (5%)
(c) List all the essential prime implicants (5%)
(d) Write the minimal SoP representation of the function. (5%)
(e) Write the minimal PoS representation of the function. (5%)

(15%)
A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = \overline{X}Y + XA$$

$$D_B = \overline{X}B + XA$$

$$Z = B$$

(a) Derive the state table (5%)
(b) Derive the state diagram (5%)
(c) Draw the logic diagram of the circuit (5%)

4. (25%)
Use T-type flip-flops to design a counter with following repeated binary arbitrary sequence F: *0,1,3,2,4,6*:

(a) Derive the state table (5%)
(b) Derive the simplified input function for the T-type flip-flops (5%)
(c) Draw the logic diagram of the circuit (5%)
(d) Design the up/down, arbitrary sequence F counter with the following table. (10%)

S1	S0	Count Mode
0	0	Up
0	1	Down
1	0	Arbitrary sequence F
1	1	Arbitrary sequence F

5. (10%)
The output of a five-input "majority voter" circuit, shown in the following figure, is to be 1 whenever a majority of its inputs is 1. Design this circuit with PLA.