所別：電機工程學系碩士班乙、丙組 科目：電子學

1. 是非題(10 分，答對每小題得 2 分，答錯每小題倒扣 1 分。請以"Yes"or "No"答題)

(1) The reverse leakage current of a p/n junction diode increases with operating temperature.

(2) The junction capacitance of a reverse-biased p/n junction diode is larger than that of the same diode under forward-bias condition.

(3) The p/n junction diode small-signal resistance r_d is proportional to the bias current I_D.

(4) The breakdown voltage of a p/n junction diode is reduced as N_A increases from 10^{16} cm^{-3} to 10^{18} cm^{-3} and N_D is fixed.

(5) Consider a CMOS inverter shown in Fig. 1. If $V_{DD} = 5$ V, $V_{tn} = |V_{tp}| = 1$V, and $2.5 \times (W/L)_n = (W/L)_p$, then both NMOS and PMOS transistors are operating in saturation region as $V_{in} = V_{out} = 2.5$ V.

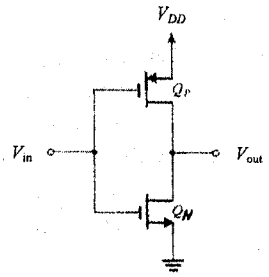

Fig. 1

2. 選擇題(10 分)

Consider the circuits (a), (b), (c) and (d) shown in Fig.2, assume that every transistor is biased in the forward-active mode and has the same $\beta_F = 100$, $V_{BE(on)} = 0.7$ V, and $V_A = \infty$. If the current sources I_1, I_2, I_3, and I_4 are adjusted such that each Q_1 transistor has the same dc collector current and hence, the same small-signal parameters.

(1) Consider the input resistance R_i, (A) $R_{ia} > R_{ib} > R_{ic} = R_{id}$ (B) $R_{id} > R_{ic} > R_{ib} > R_{ia}$ (C) $R_{id} > R_{ic} = R_{ia} > R_{ib}$ (D) $R_{ib} > R_{ia} = R_{ic} > R_{id}$. (5 分)

(2) Consider the voltage gain $A_v = |V_{out}/V_{in}|$, (A) $A_{va} > A_{vb} > A_{vc} > A_{vd}$ (B) $A_{vd} > A_{vb} > A_{va} > A_{vc}$ (C) $A_{vd} > A_{vb} > A_{va} = A_{vc}$ (D) $A_{vd} > A_{vc} = A_{va} > A_{vb}$. (5 分)

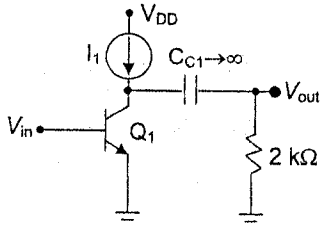

Fig. 2(a)

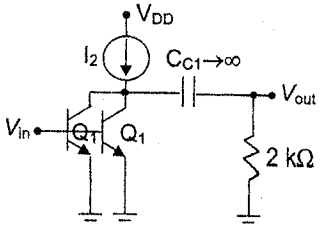

Fig. 2(b)

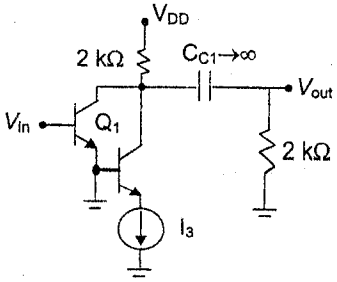

Fig. 2(c)

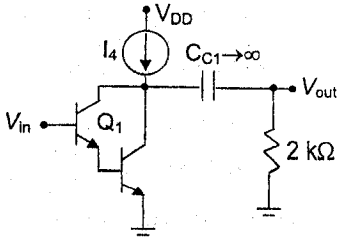

Fig. 2(d)

3. 選擇題

Analyze the high frequency response of a common source CMOS amplifier as shown in Fig. 3. The dc bias current is 100 μA. For Q_1, $\mu_n C_{ox}$=90 μA/V^2, V_A=12.8V, and W/L=100 μm/1.6 μm, and C_{gs}=0.2 pF, C_{gd}=0.015 pF, and C_{db}=20 fF. For Q_2 and Q_3, $\mu_p C_{ox}$=30 μA/V^2, C_{gd}=0.015 pF, C_{db}=36 fF, and $|V_A|$=19.2 V. There is 0.3 pF stray capacitance between the common drain connection and ground, and the resistance of the input signal generator is negligibly small. Assume the signal voltage at the gate of Q_2 is zero.

3-1 (3 points) Find g_m for Q_1: (A) 0.106 mA/V, (B) 0.053 mA/V, (C) 1.06 mA/V, (D) 0.212 mA/V, (E) 0.160 mA/V.

3-2 (3 points) Find the output resistance of the amplifier (A) 128 kΩ, (B) 192 kΩ, (C) 320 kΩ, (D) 76.8 kΩ, (E) 160 kΩ.

3-3 (4 points) Find the low frequency voltage gain A_V: (A) –203 V/V, (B) –81.4 V/V, (C) –106 V/V, (D) –135 V/V, (E) -122.1 V/V.

3-4 (5 points) Find the frequency of the zero. (A) 11.25 GHz, (B) 4.75 GHz, (C) 2.38 GHz, (D) 5.625 GHz, (E) 2.81 GHz.

3-5 (5 points) Find the frequency of the pole. (A) 24.1 MHz, (B) 2.41 MHz, (C) 550 KHz (D) 12.02 MHz, (E) 5.37MHz.

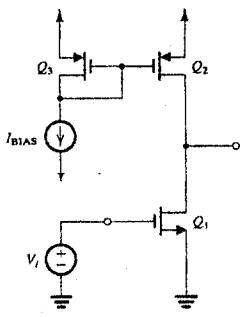

Fig. 3 Common source CMOS amplifier with a current-mirror active load.

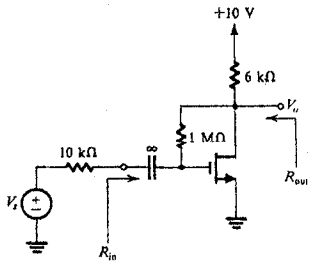

Fig. 4 Circuit for Problem 4

注意：背面有試題

所別：電機工程學系碩士班乙、丙組 科目：電子學

4. 選擇題

Negative feedback is to be used to modify the characteristics of a particular amplifier for various purposes. Identify the feedback topology to be used if:

4-1 (3 points) Both input resistance and output resistance are to be raised. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

4-2 (3 points) Input resistance is to be lowered and output resistance raised. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

A feedback circuit is shown in Fig. 4. Let the parameters of the MOSFET to be $V_t = 2$ V and $\mu_n C_{ox}$ (W/L) = 0.5 mA/ V^2.

4-3 (7 points) Find the voltage gain (V_o/V_s). (A) –2.8 V/V, (B) –8.4 V/V, (C) –11.3 V/V, (D) –6.4 V/V, (E) -5.6 V/V.

4-4 (7 points) Find the input resistance. (A) 9.34 kΩ, (B) 286 kΩ, (C) 18.68 Ω, (D) 143 kΩ, (E) 160 kΩ.

5. (20 分)

Consider the shown cascoded input stage of a CMOS op amplifier. Let $2I = 50$ μA, $I_{BIAS} = 10$ μA, $\mu_p C_{ox} = 10$ μA/V^2, $\mu_n C_{ox} = 20$ μA/V^2, $|V_t| = 1$ V, W/L for Q_1, Q_2, Q_{1C}, and $Q_{2C} = 240/8$, W/L for $Q_5 = 300/10$, W/L for Q_3, Q_{3C}, Q_4, and $Q_{4C} = 120/8$. $V_{DD} = 5$V and $V_{SS} = -5$ V.

(a) Find the required W/L ratio and V_{SD} of Q_B so that the Q_1, Q_2, Q_{1C}, and Q_{2C} are operating at the boundary of saturation region. (4 分)

(b) Find the required V_{BIAS1}. (2 分)

(c) Calculate V_{GS} for each of Q_3, Q_{3C}, Q_4, and Q_{4C}. (4 分).

(d) Find the input common mode range. (10 分).

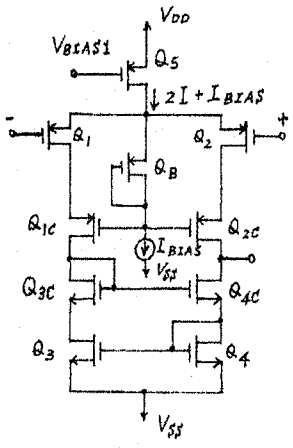

Fig. 5

6. (20 分)

Consider the shown Pierce crystal oscillator accompanied with the equivalent circuit of the crystal.

(a) If the crystal has $L = 0.052$ H, $C_S = 0.0012$ pF, $C_P = 4$ pF, and $r = 120$ Ω, find the series resonance frequency f_s, parallel resonance frequency f_p, and Q factor of the crystal. (6 分)

(b) Let C_1 be variable in the range 1 to 10 pF, and $C_2 = 10$ pF. Find the range over which the oscillation frequency can be tuned. (14 分)

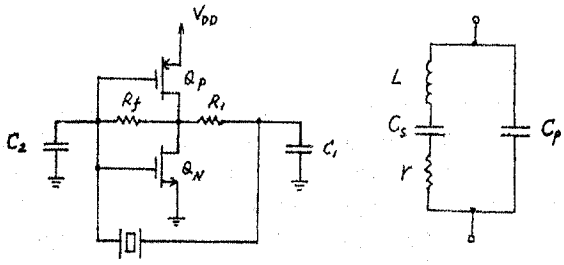

Fig. 6