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1. 計算題 (18 分)

Calculate the voltage gains (v_o/v_i) for the following circuits:

1-1 Figure 1(a) shows a folded MOS amplifier formed by cascading two common source stages. Assuming Q_1 and Q_2 have the same transconductances of 1 mA/V, bias current I = 100 μA, $V_{An} = |V_{Ap}|$ = 2 V, and the biasing current sources have an output resistance equal to that of Q_1. Find its overall voltage gain. (6 分)

1-2 The MOSFETs in the circuit of Fig. 1(b) are matched, having $\mu_n C_{ox} (W/L)_1 = \mu_p C_{ox} (W/L)_2$ = 1.0 mA/V^2, threshold voltage $|V_t|$ = 0.5 V, $r_O = \infty$, and feedback resistor R_F = 100 kΩ. Find the overall voltage gain of the amplifier. (6 分)

1-3 Figure 1(c) shows a circuit for a voltage to current converter employing an op-amp with an open circuit voltage gain A = 1000. The MOSFET Q_1 has a transconductance g_m = 1.0 mA/V, a source resistor R_S = 1 kΩ, a drain resistor R_D = 10 kΩ and $r_O = \infty$. Find its closed-loop voltage gain. (6 分)

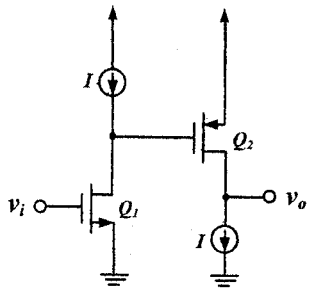

Fig. 1(a)

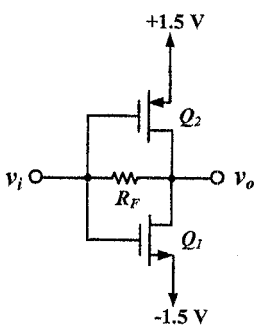

Fig. 1(b)

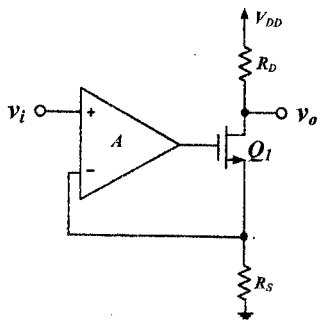

Fig. 1(c)

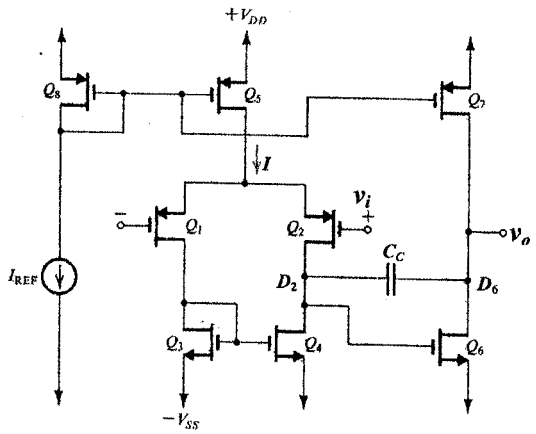

Fig. 2

2. 計算題 (18 分)

Figure 2 shows the topology of a two-stage CMOS operational amplifier. The design parameters are listed as follows: $(W/L)_1 = (W/L)_2$ = 20 μm/0.8 μm, $(W/L)_3 = (W/L)_4$ = 5 μm/0.8 μm, $(W/L)_6$ = 10 μm/0.8 μm, $(W/L)_5 = (W/L)_7 = (W/L)_8$ = 40 μm/0.8 μm, I_{REF} = 90 μA, V_{tn} = 0.7 V, V_{tp} = -0.8 V, $\mu_n C_{ox}$ = 160 μA/V^2, $\mu_p C_{ox}$ = 40 μA/V^2, $|V_A|$ = 9 V for all devices, $V_{DD} = V_{SS}$ = 2.5 V. The total capacitances between node D_2 and ground is C_1 = 0.1 pF, and the total capacitances between the output and ground is C_2 = 2 pF.

2-1 Find the dc open-loop voltage gain. (6 分)

2-2 Find the value of C_C that results in unit-gain frequency f_t = 10 MHz. And also find the corresponding frequencies of transmission zero f_Z and second pole f_{p2}. (6 分)

2-3 If a resistor R is placed in series with C_C, find the value of R to obtain the transmission zero to be located at infinite frequency. (6 分)

3. 計算題與簡答題 (14 分)

Figure 3 shows a second order filter which is realized using the op-amp RC resonator. K is the voltage gain of buffer amplifier. The design parameters of this filter are listed as follows: $R_1 = R_2 = R_3 = R_5$ = 13.25 kΩ; R_6 = 265 kΩ; $C_4 = C_6$ = 1.2 nF.

3-1 Please identify the filter type. (2 分)

3-2 What are the equivalent inductor value L and pole Q factor of the resonator? (6 分)

3-3 What are the pole frequency ω_0 and its 3-dB bandwidth of this filter? (6 分)

注意：背面有試題

4. 設計題 (10 分)

Fig. 4 shows a NMOS network of a static CMOS logic gate with five input signals A, B, C, D, E and output node F. Design and complete the full transistor circuit for this static CMOS logic gate to perform a complemented function. (10 分)

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5. 設計題 (10 分)

Design a complementary CMOS gate to perform the logic function C_i as shown in Fig. 5. (10 分)

6. 設計題 (12 分)

Figure 6 shows a multi-output domino logic circuit. Can you find out the output logic functions of C_3, C_2 and C_1? (12 分)

7. 計算題 (8 分)

Determine the dynamic power dissipated for a typical CMOS clock driver with a 3 pF capacitance loading when operated at a frequency of 400 MHz and V_{DD} is 2.5 volts. (8 分)

8. 說明題 (10 分)

Draw a PN junction cross-section view includes the electrical field, potential voltage and positive/negative charges in the junction. (10 分)

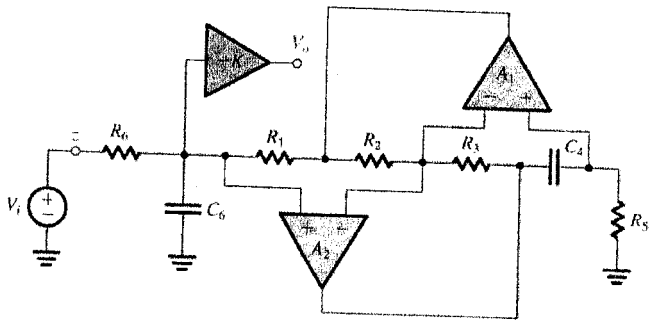

Fig. 3

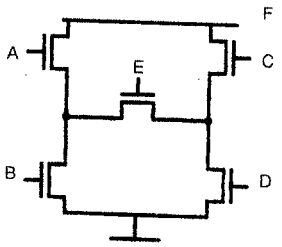

Fig. 4

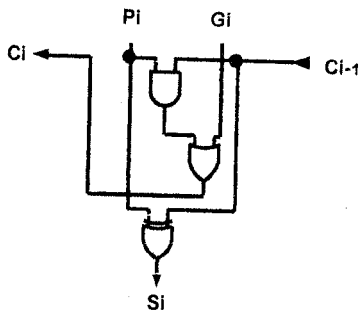

Fig. 5

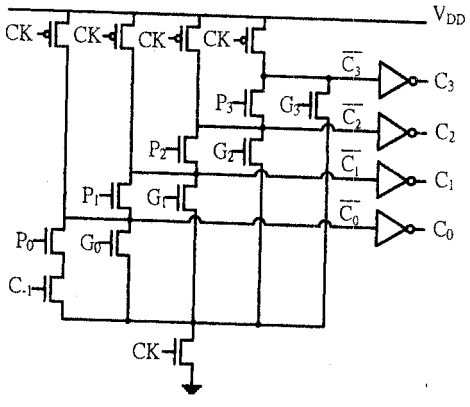

Fig. 6