國立中央大學99學年度碩士班考試入學試題卷

所別：電機工程學系碩士班 固態組(一般生)　科目：半導體元件　共 1 頁 第 1 頁

本科考試禁用計算器

＊請在試卷答案卷（卡）內作答

1. (20% = 5% + 5% + 10%) Draw the schematic energy band representations for a Si PN diode at (a) thermal equilibrium, (b) reverse bias. And (c) with built-in potential V_{bi}, calculate the total depletion layer from Poisson's equation, where N_A is accepter concentration, N_D is donor concentration, ε is Si dielectric constant.
2. (20 %) To measure the carrier concentration directly, the most commonly used method is the Hall effect. If you have a p-type Si semiconductor, draw the basic measurement setup to measure its carrier concentration. You need to show how to measure, and what concentration you get from your measurement.
3. (10% = 5% + 5%) (a) What is the main reason to induce the long transient behavior in the diode forward-to-reverse-bias transition time? (b) How to reduce a PN diode switching turn-off time?

4. (10% = 5% + 5%) An ideal MOS capacitor at 300 K has an Al gate with an oxide thickness t_{ox} on p-type Si with the metal work function $\phi_m = 4.10$ V, and the p-type substrate work function $\phi_s = 4.93$ V.
(a) Calculate the ideal flat band potential voltage V_{FB}^o.
(b) Calculate the non-ideal flat band potential voltage V_{FB} if a fixed charge $Q_f = 1 \times 10^8$ C/cm^2 located at $0.5 \times t_{ox}$. Note that the $C_{ox} = 1 \times 10^8$ F/cm^2.

5. (20% = 5% + 5% + 5% + 5%) An NMOS circuit is shown in Fig. 5(a), and A PMOS circuit is shown in Fig. 5(b).
(a) Calculate V_{DS} if $V_i = 2.0$ V in Fig. 5(a).
(b) Calculate V_{DS} if $V_i = 3.0$ V in Fig. 5(a).
(c) Calculate V_{DS} if $V_i = 2.0$ V in Fig. 5(b).
(d) Calculate V_{DS} if $V_i = 3.0$ V in Fig. 5(b).
If the solution of V_{DS} is difficult to calculate, the solution may be set in the form $V_{DS}^2 + a \times V_{DS} + b = 0$, and calculate a and b. For n-channel MOSFET, $I_D = \beta_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ in the linear region, and $I_D = \beta_n(V_{GS} - V_T)^2$ in the saturation region. Assume $\beta_n = 1$ mA/V^2, $V_{DD} = 5$ V, the threshold voltage $V_{Tn} = 1$ V, and $V_{Tp} = -1$ V. For p-channel MOSFET, the I_D can be obtained from the equations for n-channel MOSFET, and $\beta_p = \beta_n$.

6. (20% = 5% + 5% + 5% + 5%) Briefly answer the following questions.
(a) Assume an npn bipolar transistor is biased in saturation region. Sketch the minority distribution in the base region, and the energy-band diagram from emitter to collector.
(b) For an npn BJT, compare BV_{CEO} with BV_{CBO} and I_{CEO} with I_{CBO}. Which one is larger and explain the reasons. BV_{CEO} is the breakdown voltage of collector-emitter with base open, and BV_{CBO} is the breakdown voltage of collector-base with emitter open. I_{CEO} is the reverse-bias collector-emitter current with base open, and I_{CBO} is the reverse-bias collector-base current with emitter open.
(c) For an npn BJT, describe the Ebers-Moll model and the hybrid-π model.
(d) Describe a Schottky clamped transistor can be used to reduce the storage time and increase the switching speed. The Schottky clamped diode is a normal npn bipolar device with a Schottky diode connected between base and collector.

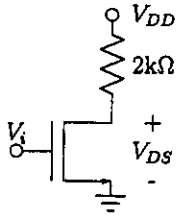

Fig. 5(a)

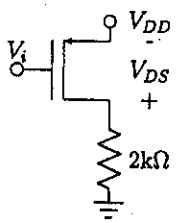

Fig. 5(b)