所別： 資工類 　　　　　　　　　　　　　　　共 7 頁 第 1 頁

科目： 作業系統與計算機組織

本科考試禁用計算器　　　　　　　　　　＊請在答案 卡 內作答

多選題（每一選項單獨計分，答錯倒扣一分）每題 5 分

1. In Boolean algebra, which of the following statements are true?
   (Note: Z' is the inverse of Z)
   (A) X+YZ'=(X+Y)(Y+Z')
   (B) (X+Y)(X'+Z)=XZ+X'Y
   (C) (W'+Z+XY)(Z'+W'+XY)=Z'+XY
   (D) (X+Y)(Y+Z)(X'+Z)=(X'+Z)(X+Y)
   (E) XY'Z+YZ=XZ+YZ

2. About single-cycle and multi-cycle implementation, which of the following statements are true?
   (A) Single-cycle implementation of CPU is used in the mainstream processors nowadays.
   (B) For single-cycle implementation of CPU, the clock cycle is determined by the longest possible path.
   (C) Single-cycle implementation of CPU allows a functional unit to be used more than once per instruction.
   (D) Compared to single-cycle implementation, multicycle implementation is more efficient.
   (E) None of the above.

3. Consider the following code sequence:
   SUB   R2, R1, R3
   AND   R4, R2, R5
   OR   R7, R6, R2
   ADD   R8, R2, R2
   SW   R9, 100(R2)
   Which of the following statements about the dependency in the code sequence are correct?
   (A) The dependency between SUB and AND instructions can be detected by the logic: EX/MEM.RegisterRd = ID/EX.RegisterRs
   (B) The dependency between SUB and OR instruction can be detected by the logic: MEM/WB.RegisterRd = ID/EX.RegisterRt
   (C) The two dependencies between SUB and ADD instructions are not hazards

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(D) There is no data hazard between ADD and SW instructions.
(E) None of the above

4. About the branch prediction, which of the following statements are true?
   (A) For a one-bit dynamic branch predictor, the branch prediction buffer contains one bit to record whether the branch instruction was recently taken or not.
   (B) A branch prediction buffer is a small special-purpose memory indexed by the higher-order bits of the address of the branch instruction.
   (C) For a two-bit dynamic branch predictor, a prediction must be wrong twice before it is changed.
   (D) The assumption of dynamic branch prediction is that the underlying algorithms and the data that is being operated on have regularities.
   (E) If the delay branch slots can be scheduled with independent instructions from before the branch, branch hazards can be avoided.

5. For the instruction set design, which of the following statements are true?
   (A) Compared to Mem-Mem architecture or Reg-Mem architecture, Reg-Reg architecture has the disadvantage of having large variation in CPI.
   (B) MIPS requires that objects must be aligned in the memory.
   (C) Register indirect addressing mode can be used for accessing using a pointer or a computed address. For example: Add R4, (R1) means that
   $Regs[R4] \leftarrow Regs[R4] + Mem[Regs[R1]]$
   (D) Modern compiler technology and its ability to effectively manipulate registers has led to a decrease in register counts in more recent architectures.
   (E) For PC-relative addressing mode, a displacement is added to the program counter.

6. Selecting items which are need to be supported by the operating system for handheld devices :
   (A) Batch programming
   (B) Virtual memory
   (C) Time sharing
   (D) Interrupt driving I/O
   (E) RAID .

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7. Some computer systems do not provide a privileged mode of operation in hardware. To construct a secure operating system for these computer systems, An OS for a machine of this type would need to remain in control at all times. This is could be accomplished by the following methods:

   (A) software interpretation of all user programs.

   (B) co-execution with co-processor to execute all programs.

   (C) networked server support to execute programs.

   (D) all programs be written in high-level languages so that all object code is compiler produced and checked.

   (E) cluster computing in database cloud system.

8. Which of the following components of program state are shared across threads in a multithreaded process?

   (A) Register values

   (B) Heap memory

   (C) Global variables

   (D) Stack memory

   (E) Local variables

9. Which of the following scheduling algorithms would result in starvation?

   (A) First-come, first-served

   (B) Shortest job first

   (C) Round robin

   (D) Priority

   (E) None

10. A system with two dual-core processors has four processors available for scheduling. A CPU-intensive application is running on this system. All input is performed at program start-up, when a single file must be opened. Similarly, all output is performed just before the program terminates, when the program results must be written to a single file. Between startup and termination, the program is entirely CPU-bound. Your task is to improve the performance of this application by multithreading it. The application runs on a system that uses the one-to-one threading model(each user thread maps to a kernel thread).

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(a). How many threads will you create to perform the input and output?

(b). How many threads will you create for the CPU-intensive portion of the application?

(A) Single thread for each input , output

(B) Two threads for each input , output

(C) Four threads for each input, output

(D) Two threads for CPU-intensive

(E) Four threads for CPU-intensive

11. Choose the correct statements from the multiple choices.

　　(A) A user-level process cannot modify its own page table entries.

　　(B) Threads can migrate between processors.

　　(C) Dirty bit is used to reduce overhead of page transfers.

　　(D) The test-and-set instruction need to be a privileged instruction.

　　(E) None of the above

12. Choose the statements that are policies (not mechanisms) from the multiple choices.

　　(A) A list of runnable processes is stored in a heap.

　　(B) Processes owned by root have higher priority than normal user processes.

　　(C) An operating system uses a timer to reclaim the cores from user processes.

　　(D) Users must change their passwords every 90 days.

　　(E) None of the above

13. Choose the correct statements from the multiple choices regarding deadlock.

　　(A) Banker's algorithm is used for recovery from deadlock.

　　(B) In Banker's algorithm, each process must declare the maximum number of instances of each resource type that it may ever claim.

　　(C) In Banker's algorithm, when a process gets all its resources it must return them in a finite amount of time.

　　(D) If a system is in an unsafe state, then there is no allocation sequence that allows the processes to finish executing.

　　(E) None of the above

單選題（答錯倒扣 2 分） 每題 5 分

14. Consider the following instruction mix for a processor.

    ALU operations: 40%, uses 4 cycles

    Branch operations: 30%: uses 4 cycles

    Memory references: 30%: uses 5 cycles

    The un-pipelined processor has a clock cycle time of 1ns. The pipelined processor
    has a clock cycle time of 1.2ns. Suppose that we ignore any latency and hazards
    and assume that the pipelined processor has an ideal CPI of 1. How much speedup
    can be achieved when comparing the un-pipelined processor and the pipelined
    processor?

    (A) 3.28

    (B) 3.35

    (C) 3.58

    (D) 3.86

    (E) 3.98

15. We know that the Boolean function F1(A,B,C,D)=AB'+CD has the minterms,
    M3,M7,M8,M9,M10,M11,M15. Now, F2(A,B,C,D)=A'B'D+CD'+A'BC'+ABD.
    X_i=i if F2(A,B,C,D) has a minterm M_i, and X_i=0, otherwise. The sum of all the
    sixteen X_i is K, $0 \le i < 16$. What is (K mod 5)? ("mod" is the modulo operation.)
    (A) 0 (B) 1 (C) 2 (D) 3 (E) 4

16. Boolean function F3(A,B,C,D)=A'B'C'+A'C'D+ABD+BCD+AC'D+AB'D'+B'CD'.
    If the number of essential prime implicants is K, what is (K mod 5)?
    (A) 0 (B) 1 (C) 2 (D) 3 (E) 4

17. Consider two different machines, A and B. The measurements on the two
    machines running a set of benchmark programs are shown below:

    Machine A (2GHz)

Instruction Type	Instruction Count (millions)	CPI
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3

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Machine B (2.2GHz)

Instruction Type	Instruction Count (millions)	CPI
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

If the MIPS of the slower machine is K, what is (Round(K) mod 5)?
(Note: Round(K)=floor(K+0.5))
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

18. A processor with 2G Hz has a base CPI of 4 when all the memory references hit in the primary memory. Assume that a main memory access time is 100 ns, including all the miss handling and that the miss rate at the primary cache is 8%. We add a secondary cache that has a 20-ns access time and helps to reduce the miss rate to the main memory to 2%. The resulting CPI now is K. What is (Round(K*8) mod 5)? (Note: K*8 means K multiplied by 8)
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

19. How many new processes are created in the below program?

```
int main(void)
{
    for (int i = 0; i < 3; i++) {
    pid_t pid = fork();
    }
    return 0;
}
```

(A) 3
(B) 5
(C) 7
(D) 9
(E) None of the above

20. How many IP addresses are available for hosts on the network 172.16.41.0/27?
(A) 2^{27}

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(B) $2^{27} - 2$

(C) 32

(D) 30

(E) None of the above