1. You are considering two alternative designs for an instruction memory: using expensive and fast chips or cheaper and slower chips. If you use the slow chips you can afford to double the width of the memory bus and fetch two instructions, each one word long, every two clock cycles. With the more expensive fast chips, the memory bus can only fetch one word every clock cycle. Due to spatial locality, when you fetch two words you often need both. However, in 20% of the clock cycles one of the two words you fetched will be useless. How do the memory bandwidths of these two systems compare? (10%)

2. A nonpipelined processor X has a clock rate of 25 MHz and an average CPI (cycles of per instruction) of 4. Processor Y, an improved successor of X, is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 20 MHz. If a program containing 100 instructions is executed on both processors, what is the maximum speedup of processor Y compared with that of processor X? (10%)

3. Compare the instruction-set architecture in RISC and CISC processors in terms of instruction format, addressing modes, registers, and CPU control. (20%)

4. Consider a cache (M_1) and memory (M_2) hierarchy with the following characteristics:

   M_1: 16K words, 50 ns access time

   M_2: 1 M words, 400 ns access time

   Assume eight-word cache blocks and a set size of 256 words with set-associative mapping. (a) Show the mapping between M_2 and M_1. (b) Calculate the effective memory-access time with a cache hit ratio of $h = 0.95$. (20%)

5. Identify the relative advantages of the synchronous bus and the asynchronous bus. (10%)

6. Define the following terms: (10%)
   (a) Wormhole routing
   (b) Systolic array
   (c) Dataflow computer
   (d) Multistage interconnection networks

7. Based on your view point, what are the future directions for computer architectures and compilers? (20%)