1 (15%) Answer the following question about performance:

a What is the Amdahl's Law?

b Given a computational task in which at most 20% portion can be parallelized, what is the maximal speedup you can obtain according to the Amdahl's Law?

c Suppose you want to achieve a speedup of 80 with a multi-processor system with 100 processors. Suppose you already have a sequential program X. Only what fraction of X can be sequential in order to achieve this goal?

2 (15%) Design a multiplier which can multiply two n-bit integers. For simplicity, you can assume the these integers are unsigned integers.

3 (25%) Consider the following DLX program, assuming that we have 5 pipelining stages of *instruction fetch, instruction decode, execution, memory read/write*, and *write-back*.

a Identify all hazards in this program.

b Show how to use data forwarding technique to resolve this problem. There should be no stalls.

c How do you connect the circuits among pipelining stages to implement the data forwarding?

d How to design the control logic for data forwarding? That is, how to check that data forwarding is necessary?

e Data forwarding usually needs a larger multiplexer in the ALU inputs. Show how this is designed.

```
ADD   R1, R2, R3      // R1 = R2 + R3
SUB   R4, R1, R5
AND   R6, R1, R7
OR    R8, R1, R9
XOR   R10, R1, R11
```

4 (25%) Answer the following questions:

a What is the result of (-6) + (-13) in 2's complement using an 8-bit code?

b (BC' + A'D)(AB' + CD')

c TTL SSI 常以 14 接腳封裝，其中 2 隻腳用來接電源，其餘可用來做爲輸出和輸出。在一個封裝內，最多可置入多少個 "三輸入的 AND 閘"?

d 欲設計二個 4-bit 數相乘的二進位乘法器，應用何種大小的 ROM 最爲經濟?

e What are denormal numbers in IEEE 754 floating-point number representation?

5 (20%) Answer the following questions.

a (5%) What is control hazard in pipeline design? Give one example.

b (5%) What are the 3 major categories for cache miss?

c (5%) What is the pseudo-associative cache technique?

d (5%) Compare page and segment in memory management.