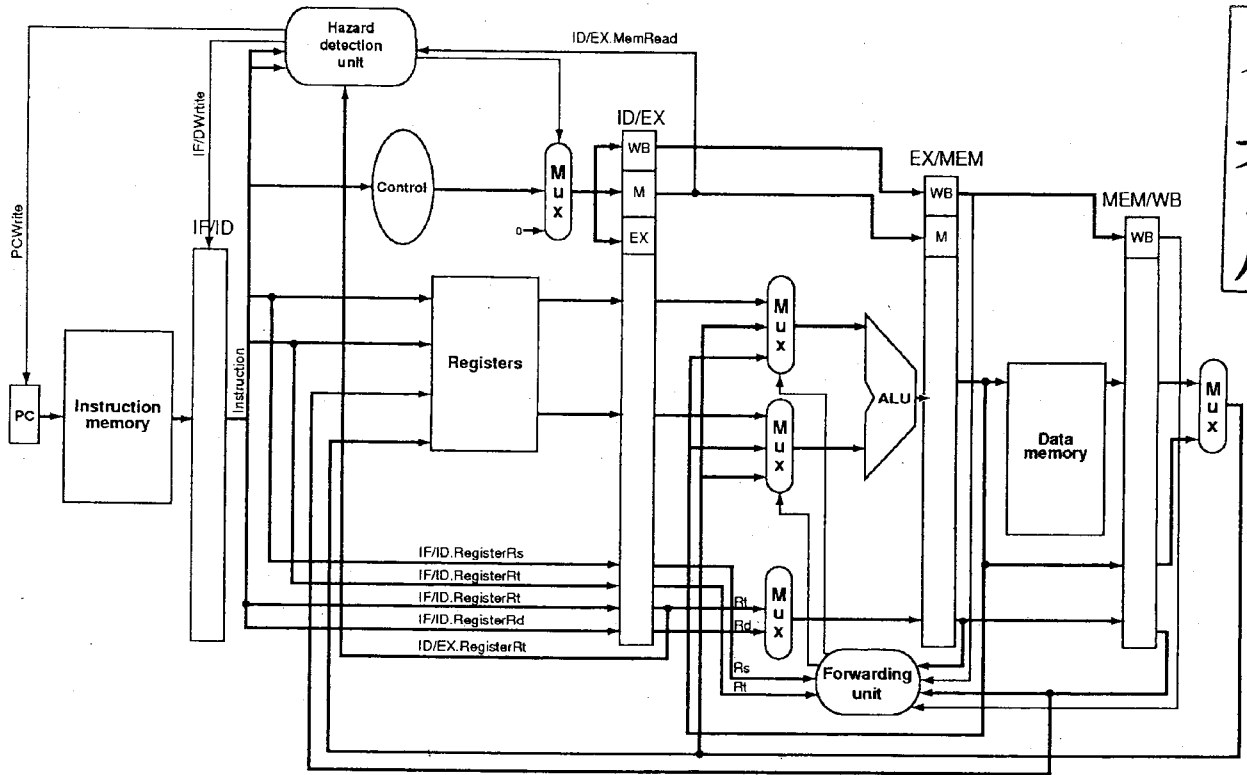


國立中央大學 97 學年度碩士班考試入學試題卷

所別：資訊工程學系碩士班 科目：作業系統與計算機組織 共 3 頁 第 1 頁
軟體工程研究所碩士班

*請在試卷答案卷(卡)內作答

1. (10%) The following figure shows a pipelining datapath with 5 stages: Instruction Fetch (IF or F), Instruction Decode (ID or D), Execution (EX or X), Memory Access (MEM or M) and Write Back (WB or W). Please answer the following questions:



參考用

- (a) (6%) Given the following instruction sequence:

```

Loop:
add $1,$2,$3    #R1=R2+R3
sub $2,$3,$1    #R2=R3-R1
lw $1,$2(0)     #Load a word from memory to R1
or $3,$2,$1     #R3=R2orR1
beq $2,$3,Loop #Branch to 'Loop' if R2=R3
addi $1,$3,2    #R1=R3+2
sw $1,$2(0)     #Store a word in R1 to memory
subi $2,$1,2    #R2=R1-2
...
    
```

If we assume that the branch decision can be made in the stage of ID and the branch is eventually taken in this case, please show the multi-cycle graph of the pipelining execution in the following form.

	CLK1	CLK2	CLK3	CLK4	CLK5	CLK6	...
add \$1,\$2,\$3	F	D	X	M	W		
sub \$2,\$3,\$1		F	D	X	M	W	
...							
add \$1,\$2,\$3							

- (b) (4%) Continue the previous question. What data hazards will be eventually solved by the hazard detection unit and what data hazards will be eventually solved by the forwarding unit in this case? Please show your answer by {instruction 1, instruction 2, register number}.

For example, {add, sub, 2}.

注意:背面有試題

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參考用

2. (15%) For the cache memory design:

- (a) (7%) Please design a 2-way set-associative cache of 8K bytes data. The block size is 2 words with 4 bytes in each word. Assume that the total cacheable physical memory is 16MB bytes. Please show the physical address format (in the order of tag, index and offset from MSB to LSB) and then the block diagram of the design, including tags, data and valid bits.
- (b) (4%) Continue the previous question. Here is a series of physical address references given as byte addresses:

Label	Memory address
A	0x235625
B	0x235627
C	0x235628
D	0x421620
E	0x422623
F	0x235627
G	0x235630
H	0x422622

Assume that the cache is initially empty and LRU replacement is adopted. Determine each reference (A~H) in the list as a hit or a miss and show the final content of the cache (i.e. the nonempty set number and the stored address range).

- (c) (4%) Assume that the virtual addresses are 32 bits long. Please describe how you will design the mapping between the virtual address and the physical address and explain why it will be more suitable to the cache that you designed above.

3. (8%) Compare the properties and architectures between SISD, SIMD, MISD and MIMD.
4. (8%) Given $x=0101$ and $y=1010$ in twos complement notation (i.e. $x = 5, y = -6$), compute step by step the product $p = x \times y$ with Booth algorithm.
5. (9%) The performance of a 100MHz microprocessor P is measured by executing 10^7 instructions of Benchmark code, which is found to take 0.25s. What are the values of CPI and MIPS for this performance experiment ?
6. (12%) Consider the following page-reference string:
 1,2,3,4,5,3,4,1,6,7,8,6,7,8,9,7,8,9,7,8,9,5,4,5,4,2
 How many page faults would occur for the following replacement algorithms, assuming four, five page frames ? Remember that all frames are initially empty, so your first unique pages will all cost one fault each.
- (a) LRU replacement
 (b) FIFO replacement
 (c) Optimal replacement
7. (16%) Prior to version 2.6 , Linux was a non-preemptive kernel . With version 2.6 the Linux kernel became fully preemptive; so a task can now be preempted when it is running in the kernel.
- (a) Describe what is the meaning of non-preemptive and pre-emptive kernel.
 (b) For single processor and multiple processors , Linux kernel 2.6 provides what mechanism for locking in the kernel ?
 (c) It provides two system calls `-preempt_disable()` and `preempt_enable()` – for disabling and enabling kernel preemption . However, in addition, the kernel is not pre-emptible if a kernel-mode task is holding a lock. To enforce this rule, what data informations of task are need to indicate the kernel can safely be interrupted, assuming there are no outstanding calls to `preempt_disable()`.
 (d) By disabling interrupts(or using spinlock) during a critical section, the kernel guarantees that it can proceed without the risk of concurrent access of shared data structures. However, there is a penalty for disabling interrupts to force any I/O device waiting for service. How Linux implements the interrupt service routine to let the kernel can complete any complex processing that has to be done in response to an interrupt without worrying about being interrupted itself.

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*請在試卷答案卷(卡)內作答

8. (12%) Assume you have a system with a static priority CPU scheduler. Assume the scheduler supports preemption. Describe what the program below prints in sequence, where the priorities are set such that T2 has a high priority, T1 has the middle priority, and T0 has the low priority. Assume the system starts with only T0 executing. Assume the semaphore mutex is initialized to 1.

```
void T0 () {
    printf ("T0-Start \n");
    StartThread (T1);
    printf ("T0-End \n");
}

void T1 () {
    printf ("T1-Start \n");
    P (mutex);
    printf ("T1-A \n");
    StartThread ( T2 );
    printf ("T1-B \n");
    V (mutex);
    printf ("T1-End \n");
}

void T2 () {
    printf ("T2-Start \n");
    P (mutex);
    printf ("T2-C \n");
    V (mutex);
    printf ("T2-End \n");
}
```

參考用

9. (10%) The Internet Protocol (IP) was designed to handle all kinds of problems in a large inter-network.
- Please briefly describe what the IP protocol does to handle the challenge that there is a cycle in the routing graph of the network.
 - Please briefly describe how Traceroute is implemented by the ICMP (Internet Control Message Protocol) packets.