1. (15 %)

Consider the BiCMOS circuit shown in Fig. 1. The bias voltage V_B is adjusted for a dc output voltage of 2 V and R_B = 1 KΩ. The transistor parameters are: $\mu_n C_{ox}$ = 60 μA/V², W = 40 μm, L = 1 μm, and V_{TH} = 0.8 V for MOSFET, and $I_S = 10^{-16}$ A, β_F = 100.

(a) Calculate the bias currents in both transistors, I_{D1} and I_{C1}.

(b) Calculate the small-signal voltage gain v_o/v_i.

(c) Find out the output resistance R_o.

2. (15%)

If the Early voltage V_A = 100 V and the common-emitter current gain $100 \le \beta_F \le 180$, $V_{BE(on)}$ = 0.7 V

(a) Please design the emitter-follower circuit (Fig. 2) (choose the appropriate values of R_1, R_2 and β_F) such that the minimum current gain $A_i = i_o/i_s = 10$.

(b) The input signal source is given by $v_s = V_m \sin w_o t$, determine the maximum value of V_m that will produce a symmetrical sinusoidal output signal.

3. (25%)

Consider the circuit shown in Fig 3, assume MOSFETs are operating in saturation region and BJTs are operating in forward active region, $\mu_n C_{ox}$ W/L = 25 mA/V² for all MOSFETs, β = 100 for all BJTs, V_T = 25 mV, $C\pi$ = Cgs = 0.5 C_{L2} << C_{L1} and $C\mu$ = Cgd << C_{L2}, neglect r_o, Ccs and Cds.

(5%) (a) The small signal DC gain of amplfier 3.a and 3.b are A1 and A2 respectively, which statement is correct ? (1) A1 > A2 (2) A1 < A2 (3) A1= A2 (答錯倒扣 2%)

(5%) (b) The phase margin of amplifier 3.a and 3.b are $\phi 1$ and $\phi 2$ respectively, $\phi 2 = 60°$, which statement is correct ? (1) $\phi 1 > \phi 2$ (2) $\phi 1 < \phi 2$ (3) $\phi 1 = \phi 2$ (答錯倒扣 2%)

(15%)(c) Assume amplifier 3.b has a 3dB bandwidth of 10kHz and a phase margin of 60°, inverting amplifier Ax has a 3dB bandwidth of 600 MHz and a small signal DC gain of -4, neglect the loading effect of Ax, what is the resulting 3dB bandwidth (5%) and phase margin (10%) of amplifier 3.c.

4. (15%)

Consider the circuit shown in Fig 4, assume V_T = 25 mV and β = 100 for Q1-Q4. (a) What kind of feedback topology (shunt-shunt, series-shunt, shunt-series, series-series) is utilized in this amplifier ? (5%)

(b) Small signal DC gain Vo/Vi = ? (10%)

5. (15%)

In the CMOS bistable circuit shown, all transistors have |Vt| = 1 V and, with k = 1/2 k' (W/L), k1=k2=k3=k4=2k5=2k6 = 200 μ A/ V², (a) Sketch and label the volatage transfer characteristic of the Q3-Q4 inverter. (5%)

(b) Sketch and label the transfer characteristic V_o versus V_i. (5%)

(c) Find the V_{IH} and V_{IL}. (5%)

6 (15%)

A particular two-input NOR gate has $t_{PHL} = 1$ ns and $t_{PLH} = 3$ ns. Five such gates, each with one input low, are connected in cascade to form a ring.

(a) Find the oscillation frequency. (5%)

(b) Two additional such gates, A and B, are connected to the ring, gate A inputs to the outputs of gates 1 and 3, and gate B inputs to the outputs of gates 1 and 4. Sketch and label the waveforms at all NOR gate outputs. (10%)

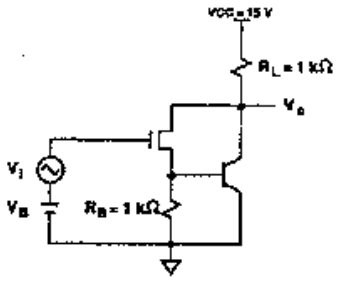

Fig 1/ Problem 1

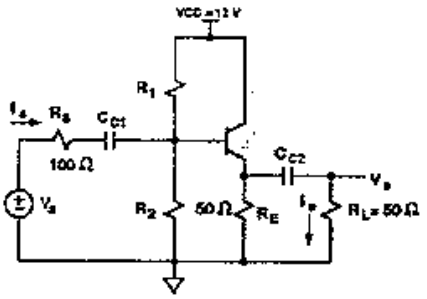

Fig 2/ Problem 2

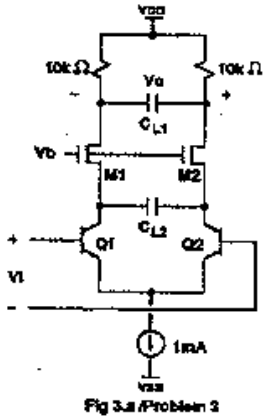

Fig 3.a /Problem 3

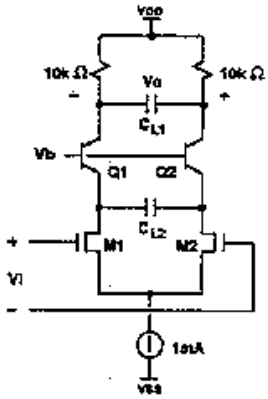

Fig 3.b / Problem 3

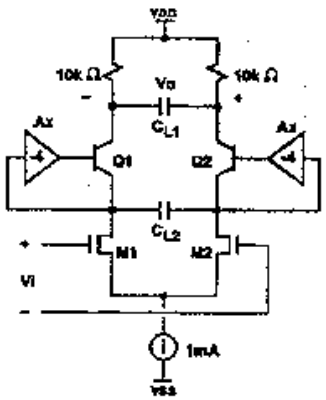

Fig 3.c / Problem 3

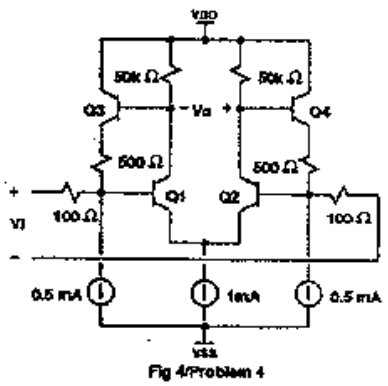

Fig 4/Problem 4

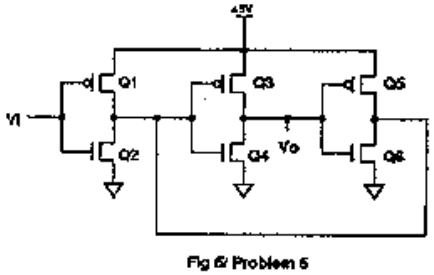

Fig 5/ Problem 5