1(a) A logic inverter modeled as in Fig.1 employs a switch for which the offset voltage is 100 mV and the on resistance is 100 Ω. If the inverter load resistance is 1 KΩ and V^+ is 5 V, what are the two expected values of the output voltage? (10分)

(b) For a particular logic family for which the supply voltage is V^+, $V_{OL} = 0.1 V^+$, $V_{OH} = 0.8 V^+$, $V_{IL} = 0.4 V^+$, $V_{IH} = 0.6 V^+$.

(1) What are the noise margins? (5分)

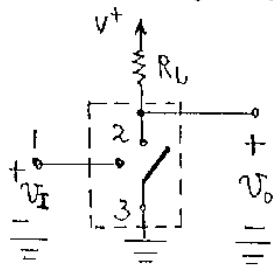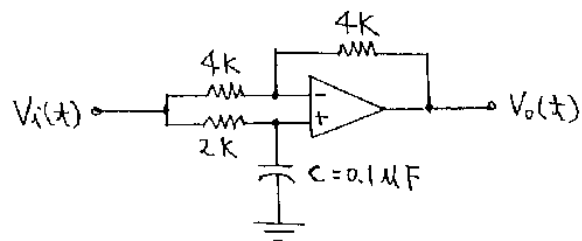(2) What is the width of the transition region (5分)

Fig. 1

Fig. 2

2. For the operational amplifier shown in Fig.2. If the input voltage $V_i(t) = 5 \sin(2 \times 10^3 t)$, to find its corresponding output voltage $V_o(t)$? (20分)

3. Consider the emitter follower circuit of Fig.3. Find the values of R_1 and R_2 which will permit a maximum possible swing in the output. (20分)
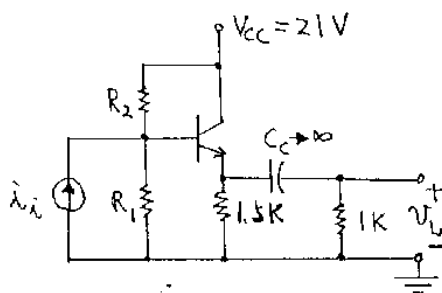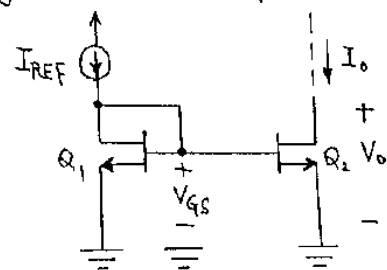

Fig. 3

Fig. 4

4. For the circuit shown in Fig.4

(a) What kind of the MOSFET Q_1 and Q_2 (i.e. P-channel or n-channel? depletion-type or enhancement-type)? Draw the physical 3 dimensional structure Q_1 (5分)

(b) Draw the $i_D - v_{DS}$ characteristics of Q_1 (5分)

(c) Derive the relation between I_o and I_{REF} (10分) [Hint: $Q_1 \neq Q_2$]

注意:背面有試題

5 Figure 5 shows the MOSFET amplifier fed with an input signal source V_i, having a negligible resistance. Using high frequency π model.

(a) To find the transfer function $V_o(s)/V_i(s)$ (5分)

(b) In practical case, zeros or poles of the transfer function is dominate? Explain it! (5分)

(c) Sketch a Bode plot for the gain magnitude. (5分)

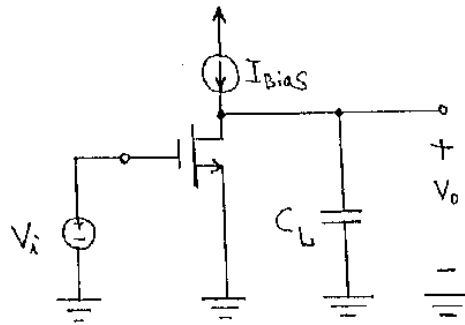(d) To find the gain-bandwidth product (5分)

Fig.5